

# **High-frequency parasitic effects in electric drives with long cables**

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## **Erklärung laut § 9 PromO**

Ich versichere hiermit, dass ich die vorliegende Dissertation allein und nur unter Verwendung der angegebenen Literatur verfasst habe. Die Arbeit hat bisher noch nicht zu Prüfungszwecken gedient.

30.11.2010,





# Preface

The present thesis represents the result of 5 year research activity as scientific assistant at the Institute of Power Electronics and Control of Drives (SRT) from Technische Universität Darmstadt. My research project was funded by the "Deutsche Forschungsgemeinschaft" (DFG) in frame of the DFG research group FOR575. I am deeply grateful to all the people who contributed in various ways directly or indirectly to my work.

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## Abstract

In the middle of the 80's the Insulated Gate Bipolar Transistor (IGBT) made its breakthrough on the market as the best compromise between the BJT and the FET, as it combines the gate structure from the FET with the bipolar structure from the BJT. Thus, it became the most popular switching device and led to an expanded use of Voltage Source Inverters for electric drives.

During the last decades, the IGBT was developed and improved considerably regarding the reduction of switching losses (faster transients) and conduction losses (lower voltage drop). This led to a further efficiency improvement of the electric converter. The faster switching transients allowed also higher switching frequencies, leading further to the reduction of losses and audible noise at electric motors. For example, the last generation of IGBTs produces voltage gradients between 5 and 10 kV/ $\mu$ s at the inverter output.

Besides these advantages, at the beginning of the 90's significant drawbacks were reported for electric drives with long cables: destroyed motor insulation, damaged motor bearings, etc. Due to the large voltage gradients and the cable-motor impedance mismatch, the traveling-wave phenomena on long cables determine voltage reflections at the motor terminals. Also, high common-mode ground currents occur, that may trigger the fault-protection systems. Finally, high values for common-mode voltage, together with high common-mode currents, lead to high bearing-current amplitudes, which eventually determine the failure of the motor bearing.

To overcome such drawbacks, "off-line" methods based on simulation models have been used since these HF parasitic effects have been reported. The electric drive may be separated in three main parts, i.e. the inverter, the cable and the motor. Usually, studies concentrate on cable and motor, strong simplifications being adopted. The inverter is replaced with a voltage source, which injects the voltage wave into the cable. In this work, the inverter is considered the source for HF parasitic effects and therefore thoroughly investigated and modeled. Also, more complex simulation models for cable and motor are developed and analyzed, together with their parameterization methods. A good compromise between model complexity and parameterization simplicity is followed. Next, all individual parts are connected together in an overall simulation model, to reflect the HF phenomena from inverter to motor.

The investigated simulation models are verified with measurements at a real setup, a process that allows the iterative improvement of the simulation models. Finally, methods for reduction of overvoltage and common-mode ground current, regarding the improvement of inverter control and the use of inverter-output / motor-input filters are investigated using the complete simulation model and the measurements at the real setup.

In the last part of the presented work, an unconventional converter topology is investigated for application with long cables, namely the Quasi-Resonant (QR) DC-link converter. Two major objectives are followed: the main issue here is the motor-friendly characteristic, leading to significant improvement of the motor operation; the secondary objective is to achieve a good efficiency compared to hard-switched converters with inverter-output filters. Finally, both objectives are validated with measurement results.



# Kurzfassung

Mitte der 80er erschien der Insulated Gate Bipolar Transistor (IGBT) auf dem Markt, der den besten Kompromiss zwischen BJT und FET Halbleitern darstellte. Der IGBT kombiniert die kapazitive Gate Struktur des FET und die bipolare Strommodulation des BJT in einem einzigen Baustein, so dass er einer der beliebtesten Halbleiter geworden ist und zu starker Ausbreitung der Spannungs-zwischenkreis-Umrichter in der Industrie führte.

IGBT wurden während der letzten Jahrzehnte bezüglich der Minderung der Schaltungsverluste (schnellere Schaltvorgänge) und der Leitverluste (kleinerer Spannungsabfall während des Leitvorganges) stark weiterentwickelt. Dies führte zur Wirkungsgradverbesserung des elektrischen Umrichters. Schnellere Schaltvorgänge ermöglichen auch höhere Schaltfrequenzen und damit Minderung der Verluste und Rauschen in elektrischen Maschinen. Die letzte IGBT Generation weist z. B. Spannungsteilheiten zwischen 5 und 10 kV/ $\mu$ s am Wechselrichterausgang auf.

Trotz der oben erwähnten Vorteile wurde Anfang der 90er Jahre von erheblichen Nebenwirkungen in umrichtergespeisten elektrischen Antrieben durch die zur Einspeisung erforderlichen langen Kabel berichtet, z.B. Zerstörung der Motorisolierung oder Beschädigung des Motorlagers. Wanderwellen auf langen Kabeln, hohe Spannungsteilheiten und Fehlanpassung der Kabel-Motorimpedanz verursachen Überspannungen an den Motorklemmen. Auch große Gleichtaktströme führen zu unerwünschter Auslösung des FI-Schutzes. Letztendlich können große Gleichtaktspannungsniveaus zusammen mit größeren Gleichtaktströmen zu hohen Lagerströmen führen, die die Zerstörung der Motorlager verursachen.

Seitdem diese HF Phänomene erkannt wurden, werden „off-line“ Methoden (basierend auf Simulationsmodelle) benutzt, um diese Probleme zu analysieren und zu vermeiden. Der elektrische Antrieb kann in drei Teile geteilt werden: Wechselrichter, Kabel und Motor. Üblicherweise werden in der Literatur Kabel und Motor zusammen vereinfacht und modelliert, während der Wechselrichter durch eine stark vereinfachte Spannungsquelle ersetzt wird, die einen Spannungspuls dem Kabel einprägt.

In dieser Arbeit wird der Wechselrichter als Quelle der parasitären HF Effekte betrachtet sowie gründlich erforscht und modelliert. Komplexere Modelle sind ebenfalls für Kabel und Motor zusammen mit deren Parametrisierungsmethoden analysiert und entwickelt. Ziel dieser Arbeit ist, einen guten Kompromiss zwischen Komplexität des Modells und einfacher Parametrisierungsmethoden zu finden. Zunächst sind alle einzelnen Teile eines elektrischen Antriebes in einem einzigen Simulationsmodell verbunden, welches letztendlich durch den Vergleich mit Messungen am Prüfstand bestätigt wird. Dadurch können iterative Verbesserungen für Modelle erreicht werden.

Weiterhin werden Minderungsmethoden bezüglich der Überspannung an Motorklemmen und des Gleichtaktstromes analysiert, die am Wechselrichter (Änderung des Spannungsprofils) und am Kabel (Einsatz von Wechselrichterausgang/Motoreingang Filtern) greifen. Dafür ist das Gesamtsimulationsmodell einzusetzen. Diese Simulationsergebnisse sind ebenfalls durch Messungen am Prüfstand bestätigt.

Der zweite Teil der vorliegenden Arbeit beschäftigt sich mit dem Einsatz von unkonventionellen Umrichtern in elektrischen Antrieben mit langen Kabeln, den

sogenannten Quasi-Resonanten Zwischenkreisumrichtern. Zwei Ziele stehen dabei im Vordergrund: erstens soll der QR-Umrichter motorfreundlich sein, d.h. die parasitären HF Effekte müssen möglichst viel reduziert werden; zweitens soll ein guter Wirkungsgrad erreicht werden, im Vergleich zu hart geschaltetem Wechselrichter + Ausgangsfilter. Am Ende werden beide Ziele durch Messungsergebnisse bestätigt.

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## List of symbols

$a, b, h_i$	: Typical cable dimensions, aux. coefficients	$e$	: Electron charge
$A_{GD}$	: Junction's surface	$\varepsilon_0$	: Air electric permittivity
$\alpha_R, \alpha_L$	: Proportionality constant for ladder circuit parameter variation	$E_{crit}$	: Critical value for electric field
$\beta$	: Traveling wave phase constant, "2 Step Rise" delay	$eq$	: Subscript – equivalent quantity
$C$	: IGBT's Collector connection	$\varepsilon_{Si}$	: drift-layer's electrical permittivity
$C_1, C_2, C_0$	: Cable's partial capacitances	$f, \omega$	: Frequency in Hz, $\text{sec}^{-1}$
$C_A, C_B, C_C$	: Equivalent measured capacitances	$f_0, \omega_0$	: Resonance frequency in Hz, $\text{sec}^{-1}$
$C_{Add}$	: Auxiliary capacitance for voltage balancing	$f_{co}, \omega_{co}$	: Cutoff frequency in Hz, $\text{sec}^{-1}$
$C_{CE}$	: Collector-emitter stray capacitance	$G$	: IGBT's Gate connection
$C_{DC-link}$	: Total DC-link capacitance	$G(s)$	: Filter's transfer function
$C_{diff\_IGBT/D}$	: IGBT / anti-parallel diode diffusion capacitance	$I, V_F$	: Forward current and voltage for anti-parallel diode
$C_{Dj}$	: junction capacitance of the anti-parallel diode	$I_B$	: Base current
$C_{ech\_i-0}$	: Cable equivalent capacitance – conductor $i$ to shield (ground)	$I_{C/G}$	: IGBT's collector/gate current
$C_{Elko}$	: Capacitance of electrolytic capacitor	$I_{CM/DM}$	: Common/differential mode current
$C_{GC/GE}$	: Gate-collector/emitter stray capacitance	$I_D$	: MOSFET's drain current
$C_{GS/GD}$	: Gate-source/drain stray capacitance of IGBT's internal FET	$I_{D\_Tail/D\_Tail0}$	: Current sources for tail current/initial tail current value (anti-parallel diode)
$C_{ies/oes}$	: IGBT's input/output stray capacitance	$I_{FET}$	: IGBT's collector current component flowing through FET
$C_{junct.}$	: <b>pn</b> junction capacitance	$I_{in/ref}$	: Incident / reflected current
$C_{OX}, C_M$	: IGBT's gate oxide stray capacitances	$I_O, I_{OX}$	: Actual and next DC-link currents
$C_{res}$	: Motor's stray capacitance to ground	$I_P$	: Peak value of resonant current
$C_{s\_i}$	: Interturn capacitance	$I_{PNP}$	: IGBT's collector current component flowing through BJT
$d$	: Distance between two neighbor conductors	$I_{Tail/Tail0}$	: Current sources for tail current/initial tail current value (IGBT)
$D$	: Discriminant	$I_{Tp1}, I_{Tp2}, I_{tp1}, I_{tp2}$	: Trip currents for resonant operation
$D_{DC+}, D_{DC-}$	: Anti-parallel diodes for DC-link switches	$I_{Trans}$	: Transfer characteristic current source
$D_{Diode}$	: Output characteristic nonlinear diode for anti-parallel diode	$\varphi_i$	: Conductor's potentials ( $i = 1 \div 3$ )
$d_i, D$	: Diameter of conductor, shield (cable)	$K_{L/S}$	: Reflection coefficient at load/source side
$D_{Out}$	: Output characteristic nonlinear diode	$k_R, k_L$	: proportionality factors for ladder circuit parameter variation
$\Delta R, \Delta L$	: Resistance, inductance difference between two freq.	$\lambda$	: Traveling wave length
$D_R, D_{R1}, D_{r1}, D_{r2}$	: Anti-parallel diodes of the resonant switches	$L', C', R', G'$	: Cable's $\Gamma$ section parameters per unit length
$D_{Trans}$	: Transfer characteristic freewheel diode	$l, l_{total}$	: Cable length
$dV/dt$	: Voltage slope	$L_A, L_B$	: Equivalent inductances between two closed and distant conductors
$E$	: Electric field	$L_{C/E}$	: Collector/Emitter side stray inductance
$E$	: IGBT's Emitter connection	$L_{CE1/CE2}$	: Distributed internal stray inductances
		$L_{CM/DM}$	: Common / Differential mode stator inductance
		$l_{crit}$	: Critical value for $\Gamma$ section length

$L_{E(C)1(2)\sigma}$	: Emitter (Collector) side distributed stray inductances for IGBT	$R_{fe}$	: Motor's iron losses
$L_{G\_int}$	: Internal gate side stray inductance	$R_G$	: External gate resistance
$L_{ij}, M_{ij}, L_{i\_HF(LF)}, C_{ij}$	: Cable's distributed parameters per unit length ( $i = 1 \div 3; j = 0 \div 3$ )	$R_{G\_in}$	: Gate-emitter input impedance
$L_M$	: Motor's main inductance	$R_{G\_int}$	: Internal gate side stray resistance
$L_{ph\_LF/HF}$	: Phase inductance at LF/HF between two conductors	$R_i, L_i, C_{i0}$	: Motor's $\Gamma$ section parameters per unit length
$L_r, L_R, C_R, C_S$	: Passive elements from resonant circuit	$R_{JFET}$	: IGBT's JFET resistance between two adjacent cells
$L_{\sigma\_DC-link}$	: DC-link stray inductance	$R_{mes\_oi}, L_{mes\_oi}$	: Measured resistance and inductance at frequency $i$
$L_{srt}$	: Motor's stray inductor in stator	$R_{MOS}$	: MOS channel resistance
$L_{TOT}$	: Total internal stray inductance of IGBT	$R_{res}$	: Coupling stray resistance of the motor winding to earth (CM path)
$\mu_0, \mu_r$	: Absolute and relative magnetic permeability	$R_{thy}$	: $p^+$ body substrate resistance
mes.	: Measured quantity	$s$	: Complex operator in Laplace transform
$M_{ij}$	: Mutual inductance between two phases	$S_{DC+}, S_{DC-}$	: DC-link switches
$N$	: Electrons concentration, region with negative carriers	sim.	: Simulated quantity
$N$	: Order number, filters proportionality factor	$S_{INV}$	: Equivalent switch for inverter bridge
$n^+$	: Region with high electrons concentration	$S_{r1}, S_{r2}, S_R$	: Resonant switches
$n^-$	: Region with low electrons concentration	$SW_{IGBT/Diode}$	: IGBT / anti-parallel diode of the auxiliary switch
$N_D$	: Electron concentration	$T, T_{osc}$	: Period of traveling wave
$N_s$	: Number of turns per phase	$T_0$	: Resonance period
$P$	: Holes concentration, region with positive carriers (holes)	$\tau_{Cr}$	: Carrier life time
$p^+$	: Region with high holes concentration	$t_{MP}$	: Main-pulse time interval
$P_{cond}$	: Conduction losses	$t_p$	: Wave propagation time along the cable
$P_{R\_F}$	: Filter's resistance losses	$t_{Pre/Post-P}$	: Pre and post-pulse time interval
$P_{RF\_D}$	: Filter's resistance + diode losses	$t_r$	: Rise time of traveling wave
$P_{sw}$	: Switching losses	$t_{SC}$	: Short-circuit time interval
$\theta$	: Angle	$\tau_{Tail}$	: Tail current time constant
$Q_i$	: Partial electric charge ( $i = 1 \div 3$ )	<b>V, K, Q, C</b>	: Voltage, coefficient, electric charge and partial capacitances matrices
$Q_{rr}$	: Reverse-recovery electric charge	$V_C$	: Speed of traveling wave
$R/L/D_{Tail/D\_Tail}$	: Components of tail current auxiliary circuit for IGBT/anti-parallel diode	$V_{CC}$	: Constant voltage source
$R_A, R_B$	: Equivalent resistances between two closed and distant conductors	$V_{CE/GE}$	: IGBT's collector/gate-emitter voltage
$R_B$	: Base resistance	$V_{CM/DM}$	: Common/differential mode voltage
$R_{C/E}$	: Collector/Emitter side stray resistance	$V_{CS}$	: ESBT's collector-source voltage
$R_{CC'+EE'}$	: Bond wires stray resistance	$V_D$	: Diffusion potential
$R_{cu}$	: Motor's core losses	$V_{DC}$	: DC-link voltage
$R_{desc}, R_{damp}$	: IGBT auxiliary resistances	$V_{DS}$	: MOSFET's drain-source voltage
$R_{drift}$	: Drift region resistance	$V_f, V_b$	: forward and backward traveling voltage waves
$R_{DS}$	: MOSFET drain-source resistance	$V_{GE\_th}$	: IGBT's threshold gate-emitter voltage
$R_{eq\_oi}, L_{eq\_oi}$	: Equivalent resistance and inductance at frequency $i$	$V_{in/ref}$	: Incident / reflected voltage
$R_F, L_F, C_F$	: Filter parameters	$V_{inv/mot}$	: Inverter output / motor terminals voltage
		$V_{inv\_sim/mes}$	: Simulated / Measured voltage at inverter output
		$V_T$	: Thermal semiconductor voltage

$w_1, w_2$	: Primary and secondary number of windings
$w_j$	: Width of space charge region
$W_{\text{Pre/Post-P}}$	: Energy saved during pre and post-pulse
$X$	: Factor for determine of $\Gamma$ section critical length
$\zeta$	: Derating factor for proximity effect, damping constant for filters
$Z_C$	: Cable characteristic impedance
$Z_{\text{cab\_CM/DM}}$	: Cable's phase impedance in CM/DM configuration
$Z_{\text{CM/DM}}$	: Common / Differential mode stator impedance
$Z_{L/S}$	: Load (motor)/source (inverter) characteristic impedance

## List of abbreviations

A/D	: Analog to Digital converter	IGBT	: Insulate Gate Bipolar Transistor
AHDL	: Altera Hardware Description Language	IM	: Induction Motor
AMI	: Antrieb Module Interface	ISR	: Interrupt Service Routine
ASD	: Adjustable Speed Drives	JFET	: Junction Field Effect Transistor
BJT	: Bipolar Junction Transistor	KCL	: Kirchhoff Current Law
BNC	: Bayonet Neill Concelman connector	KVL	: Kirchhoff Voltage Law
BVR	: Bearing Voltage Ratio	LUT	: Latch-Up Transistor
CM	: Common Mode	MOSFET	: Metal-Oxid Semiconductor Field Effect Transistor
CPLD	: Complex Programmable Logic Device	NPT	: Non Punch Through IGBT type
D/A	: Digital to Analog converter	PCB	: Printed Circuit Board
DCG	: DC Generator	PCI	: Peripheral Component Interconnect bus
DM	: Differential mode	PE	: Protective Earth
DSP	: Digital Signal Processor	PMSM	: Permanent Magnet Synchronous Motor
DSC	: Direct Self Control	PT	: Punch-Through IGBT type
EDM	: Electrostatic Discharge Machine	PWM	: Pulse Width Modulation
EMC	: Electro-Magnetic Compatibility	QR	: Quasi-Resonant
EMI	: Electro-Magnetic Interference	RTAI	: Real Time Application Interface
ESBT	: Emitter Switched Bipolar Transistor	RTM	: Real Time Module
ESL	: Equivalent Series Inductance	RT-OS	: Real Time Operating System
ESR	: Equivalent Series Resistance	SCR	: Space Charge Region
FEM	: Finite Element Method	SDRAM	: Synchronous Dynamic Random Access Memory
FET	: Field Effect Transistor	SiC	: Silicon Carbide
FOC	: Field Oriented Control	SMPS	: Switched-Mode Power Supply
FPGA	: Field Programmable Gate Array	SPT	: Soft Punch-Through IGBT type
FS	: Field-Stop IGBT type	SS	: Soft Switching
FZI	: FahrZeug Interface	SSRAM	: Synchronous Static Random Access Memory
GDU	: Gate Drive Unit	VSI	: Voltage Source Inverter
GTO	: Gate Turn-Off thyristor	WBJT	: Wide-base Bipolar Junction Transistor
GUI	: Graphic User Interface	ZCS	: Zero Current Switching
HF	: High Frequency	ZVS	: Zero Voltage Switching
HS	: Hard Switching		
IEC	: International Electrotechnical Commission		

# 1 Introduction

The electric drives are common applications for the electric-to-mechanical energy conversion. They are widespread in industry and home appliances.

The simplest electric drive consists of an electric motor connected directly to the main supply grid, usually using a power switch. Thus, only one point of operation can be achieved, determined by the poles number of the motor and frequency of the alternating-current supply, e.g. 230 V-50 Hz mains supply in Europe and 110 V-60 Hz in USA. Such examples of simple electric drives may be found in applications like fans, pumps with constant speed, simple household devices etc.

However, there are situations where a variable speed is required, making the use of Adjustable Speed Drives (ASD) necessary. This can be achieved in two ways: a) by variable mechanical coupling using gearboxes or b) using electric converters. The first solution obtains variable torque and speed from a constant speed of the electric machine shaft by different mechanical coupling ratios, manually selected by a human operator or automatically adjusted. Typical configuration for such a drive is: a central main drive and many mechanical transmission elements (fixed / variable ratio gear, differential gear, cam disc, etc.). They are high scalable but have low efficiency, low maintainability and high cost due to the many elements of mechanical transmission [1], [2].

The second solution requires power electronics (electric converters) for the energy conversion between supply mains and motor. The electric converters do not contain mechanical parts and the electric power is transformed using power semiconductors (state of the art represents the self-commutated devices). Regarding the intermediate energy storage, two types of converters can be distinguished: converters without internal energy storage, e.g. matrix converters, and converters with internal energy storage [3], respectively. From the latter, the most used in practice are the DC-link converters, where one of the alternating input quantities (current or voltage) is first transformed into a constant quantity and then into an alternating quantity with variable amplitude and frequency. Depending on the quantity used in the intermediate circuit, the following types may be distinguished: current-fed converters, where the constant current is obtained using a large inductor in the intermediate circuit; voltage-fed converters where the constant voltage is assured by large capacitors in the intermediate circuit; Z-source converters where the intermediate circuit is composed by crossed linked inductors and capacitors [3].

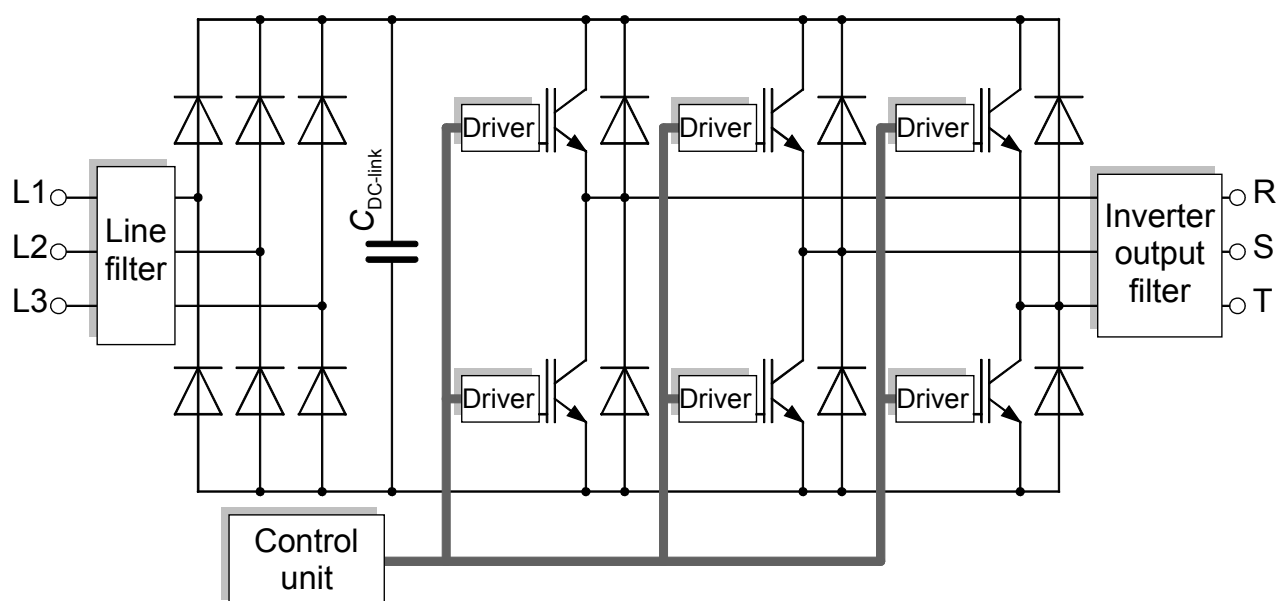
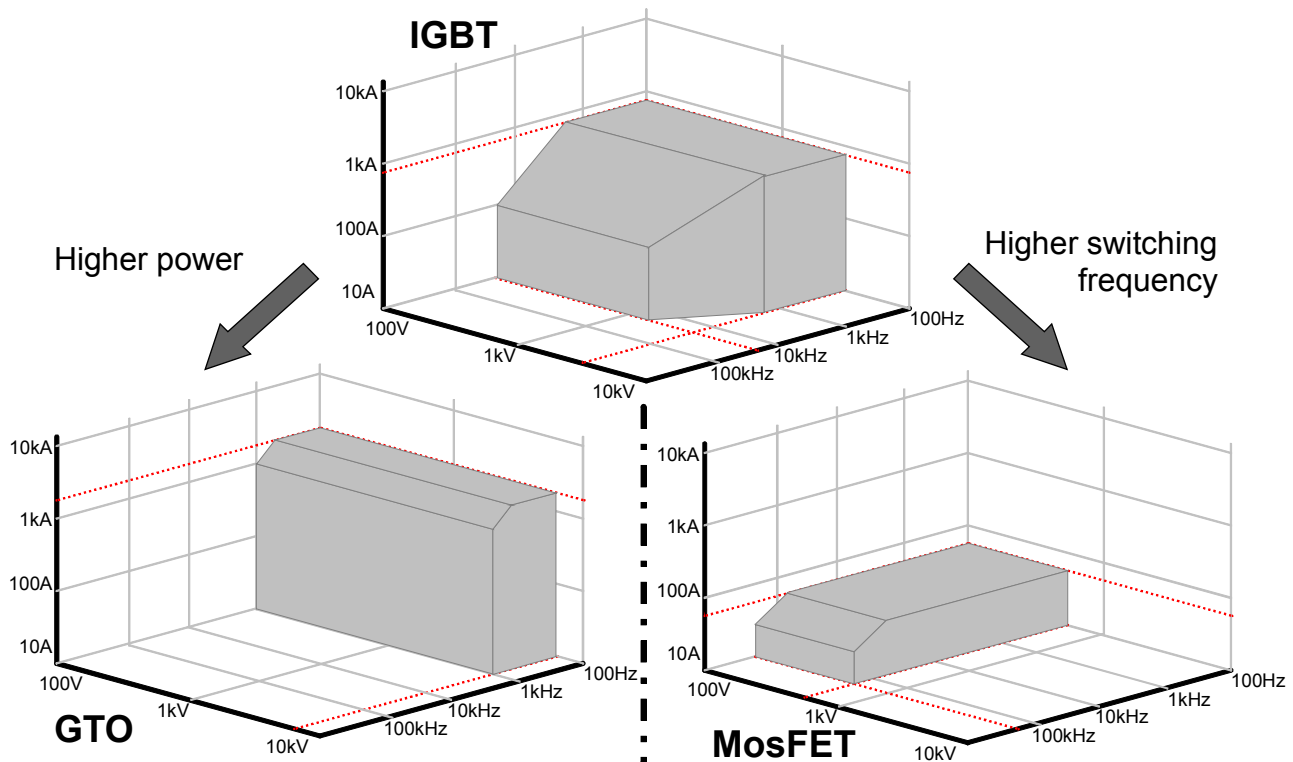


Figure 1.1: Topology of a standard voltage source converter



**Figure 1.2: Semiconductor device variations regarding switching frequency and voltage level**

Most common used in industry are the DC-link voltage-fed converters, like Figure 1.1 shows. If no regenerative braking is required, a diode bridge rectifies the input voltage, which is then filtered by the DC-link capacitor  $C_{DC-link}$ . The constant quantity is in this case the voltage and a DC-link capacitor bank is used as an energy buffer.

Next, a Voltage Source Inverter (VSI), consisting of semiconductor switches connected together like in Figure 1.1, transforms the constant voltage into an alternating one with variable frequency and amplitude. Thus, variable frequency and amplitude is obtained by modulating the width of switching pulses, a technique also known as Pulsed Width Modulation (PWM) [4]. If the operating power is higher, e.g. electric traction vehicles, the voltage level in DC link is higher. Because the switching semiconductors have a fixed breakdown voltage, more switching voltage levels are used in multi-level VSI [3].

The main parameters of semiconductor devices are switching frequency and breakdown voltage level (power), like Figure 1.2 shows. While for high-power levels, the semiconductors have slow switching transients leading to relative low switching

**Table 1.1: Switching semiconductor devices**

Semiconductor device	Advantages	Disadvantages	Operational switching frequency
Gate Turn-Off thyristor (GTO)	- high current density - high breakdown voltage - turn-off control	- low switching frequencies	Up to 1 kHz
Bipolar Transistors	- low conduction losses - medium breakdown voltage	- complex gate circuitry	Up to 100 kHz
Field Effect Transistors (FET)	- high switching frequencies (small switching losses) - simple gate circuitry	- low breakdown voltage - high conduction losses	Up to 200 kHz
Insulated Gate Bipolar Transistors (IGBT)	- simple gate circuitry - medium breakdown voltage	- medium switching frequencies	Up to 20 kHz

frequencies, at low-voltage levels the operable switching frequency is relative high.

During the years, developments in switching semiconductors led to the switching-device families summarized in Table 1.1, which can be used in VSI. Of course the presented semiconductors are used in specific applications depending on their properties. For example, the Thyristors are presently used in High Voltage DC Transmission Systems, as they require high-power density and less switching ability. Though, fast switching semiconductors like FETs are required in low-voltage applications with high efficiency, e.g. DC-DC converters, Switched Mode Power Supplies (SMPS), etc.

Because the electric converters are designed to drive the motors, they have to be adjusted to the load characteristic, i.e. inductive loads like stator coils of an electric machine. The variable voltage at the converter output is built of voltage blocks, whose width is variable. Thus, controlling the switching times, the voltage average value is also controlled following a fundamental wave [4]. Having pulsed voltages applied to the inductive load, the current will add a ripple to the fundamental waveform.

However, the load current ripple will introduce undesired harmonic losses in the cores, which carry the flux. Modern electric drives use increased switching frequencies to reduce the load current ripple and to approximate the sinus fundamental wave better, leading further to reduced harmonic losses in the machine. Moreover, it is well known that the switching transients produce an acoustic noise in the iron sheets of the core laminations, which is uncomfortable for the human ear. Increasing the switching frequency above 6 kHz leads to a considerably reduction of the audible noise [9]. A second aspect regards the energy efficiency of the inverter itself. Lower inverter losses can be achieved using the modern semiconductor devices with less switching and conduction losses. Thus, important improvements have been achieved during the last decades to decrease the switching transient times of the semiconductor devices. Also, faster semiconductor devices allow the use of higher switching frequencies for the same efficiency.

A special interest in this work represents the IGBT, as it is the most spread technology used presently in electric converters for industry applications. Its transient times decreased, e.g. currently the third generation of IGBTs achieving 50 ns rise times (voltage gradients between 5 and 10 kV/ $\mu$ s), when compared to the first generation, from mid 80's (the years of the commercial break), which possessed rise times of app. 400 ns [5].

From the entire family of electric drives with VSIs, a particular category represents the one, which uses long cables between the power electronic and the motor. Such types of ASD are found in applications where the motor has to be situated far from the electric converter, either due to the accessibility or due to the dangerous operation environment. Such an example is the speed control of the pumps in mining stations or petrochemical plants (here the converter must be located outside the explosion zone).

## **1.1 HF parasitic effects in electric drives with long cables**

The use of fast switching IGBTs in electric drives with long cables has introduced a new problem. Due to the short rise time of voltage and current, high-frequency (HF) parasitic effects occur, that may disturb the drive functionality or even damage the entire drive [6], [7]. Furthermore, IEC standards stipulate limited voltage gradients at the inverter output when long cables are used, as published in [8]. The main effects will be presented further.

### **1.1.1 Overvoltage at motor terminals**

An important parasitic effect of using fast switching semiconductors with long cables is the voltage reflection at the motor terminals, due to the impedance mismatch between cable and motor. This impedance mismatch is predominant at the electric motors with low-power levels ( $< 10$  kW), as their stator has a higher impedance than those of medium and high-power motors. This effect was reported in the literature in the early 90's when IGBT semiconductor devices were introduced in electric drives: [6], [9] and [7], [10].

Voltage overshoot will occur at the motor terminals when the incident wave is not totally absorbed due to the impedance mismatch. When the inverter output voltage rises more rapidly than the traveling period of the impressed voltage wave along the cable, voltage overshoot will be doubled. Following reasons that lead to an overvoltage occurring at the motor terminals have been identified: cable length, matching factor of the cable-to-motor surge impedance, magnitude and rise time of the PWM output voltages [11]. From these, the first two depend directly on the dimensions of the application and are fixed. Especially for low-power applications, the impedance matching factor tends to one ( $K_L \approx 1$ ). The last factor is predominant and depends on the electric converter. Therefore, many overvoltage reduction methods deal with the reduction of voltage rise time.

Specific situations have been also reported, where certain modes in PWM cycle, combined with long cable lengths, lead to voltage amplitudes greater than 2 per unit (pu.) and up to 3 or 4 pu. [12]. This happens when the last cable transient has not fully decayed before the next pulse from the inverter is applied to the cable, so that a residual trapped charge still exists on the cable. In this case, the switching frequency of the carrier, together with the modulation technique, has a predominant effect on the motor overvoltage. Another factor, that influences the  $> 2$ pu voltage magnitudes, represents the cable losses. In other words, the cable AC damping resistance influences the amount of residual charge trapped on the cable before the next inverter pulse occurs.

A more detailed analysis of the motor overvoltage phenomena is offered in chapter 2, section 2.2.1, where the transmission line theory (equations + bouncing diagram) is used to model the traveling voltage waves along the cable and the generation of motor terminal / inverter output voltages from the incident and reflected waves at different time instants.

### **1.1.2 Uneven voltage distribution on stator windings**

The motor winding can be regarded as an equivalent circuit per turn, consisting of inductance per turn, line-to-earth capacitance between conductor and stator iron, and series capacitance between conductors of adjacent turns in a slot [13]. The line-to-earth capacitance is defined by winding insulation properties and slot surface. However, the series capacitance is determined, especially for low-power motors, only by the enamel of the copper wire.

When voltage surges are applied to the motor winding, the distributed elements will determine a nonlinear voltage distribution along the motor armature. According to transmission line theory, voltage oscillations will occur with frequency determined by the winding parameters. The voltage distribution, immediately after the surge, depends on the ratio of the series capacitance (between winding turns) and line-to-earth capacitance (between conductor and stator iron) [14]. Due to small conductor surface, but big slot surface, usually line-to-earth capacitance is much higher than inter-turn capacitance. Thus, a strongly nonlinear voltage distribution between first stator coils occurs, that may lead to dangerous partial discharges of corresponding capacitances and finally damage of the insulation layer. To prevent this, better winding insulations are strongly recommended in electric drives with long cables. Moreover, certain standards have been developed in industry that set limits for voltage overshoot and voltage gradient at motor terminals, in order not to influence the motor isolation lifetime, e.g. in [8] are the overvoltage at 1000 V and voltage slope  $dV/dt$  at 500 V/ $\mu$ s limited.

### **1.1.3 Common-mode (CM) ground current**

Steep voltage pulses produce at motor terminals a displacement current to earth, mainly determined by winding-to-stator iron capacitance. Thus, the CM ground current is generated, following the path from inverter through the cable, the motor stator windings, then mainly through the winding-to-stator iron capacitance to the motor frame and partly back to the inverter housing through the cable ground connection, see Figure 1.3. Another



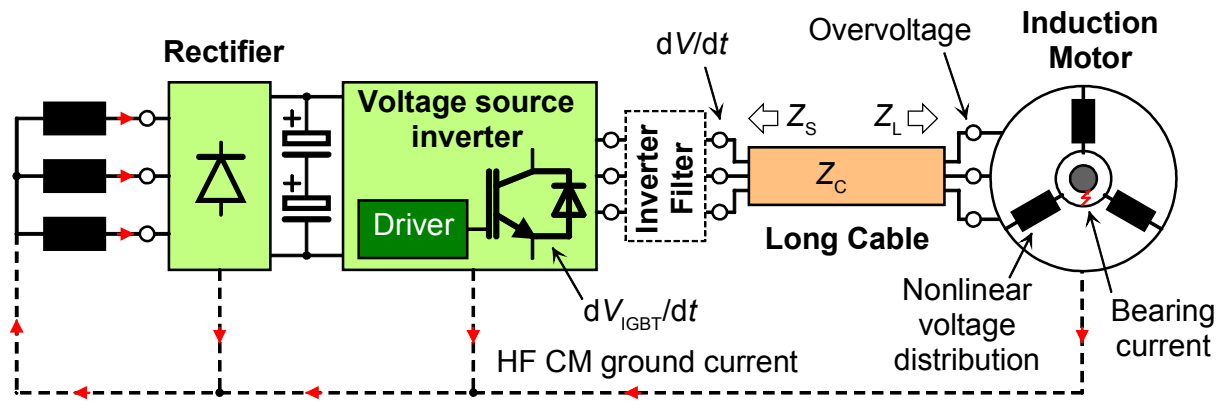


Figure 1.3: Electric drive with long cable overview and HF parasitic effects

part of the current may flow through the grounding system of the plant to the feeding transformer, where the neutral of the star connected low-voltage side (400V) is typically grounded. From this feeding transformer, the common-mode current flows back via AC-distribution to the (diode-) rectifier and the VSI.

The effects of increased CM ground current are: electromagnetic interferences with electronic equipment, interference with the ground fault protection systems in industrial facilities and induction of HF circulating bearing currents, especially in large motors, which may lead to bearing failures [15]. Therefore, the analysis of CM ground current effects needs reliable models for cable and motor to be developed for accurate estimations.

Measures for the CM ground current mitigation have been widely analyzed and proposed in literature using CM filters (chokes) [18] [19], unconventional PWM techniques [20], improved cable arrangements [21] or motor configurations [22]. Generally, they are closely related to motor overvoltage reduction and therefore, often treated together.

#### 1.1.4 Motor bearing currents

Magnetic asymmetries in electric motors produce a parasitic AC magnetic flux linkage in the loop “stator housing – drive-end bearing – motor shaft – non drive-end bearing” that induces a voltage in this loop. Only if this voltage surpasses a certain threshold level to bridge the insulating lubrication film of the bearing, a circulating bearing current may flow in the above-mentioned loop. This current, also called “classical” bearing current [16], is increasing with the motor size as the parasitic flux linkage increases also. This type of bearing currents occurs also for line-operated induction motors with two poles because they exhibit the biggest flux per pole for a certain shaft height.

Besides the “classical” type, additional bearing current types were identified for the inverter-operated motors through long cables [16]. To better understand the bearing current phenomena, the bearing functionality should be first known: during its operation, the bearing poses two types of behavior, i.e. two types of impedances between outer and inner ring: capacitive behavior occurs at high speeds and low temperatures when the lubrication acts as a dielectric); resistive behavior occurs at low speeds and/or high temperature when lubrication film is no longer homogenous and the metal contact between bearing races and balls short-circuits the dielectric.

**a) capacitive bearing currents** – divided by the bearing voltage ration (BVR), the CM voltage determines a voltage drop between inner and outer bearing races. Thus, depending on the bearing behavior, a capacitive or resistive current will occur. However, this current was found harmless for bearings due to its small amplitudes (< 200 mA) [16];

**b) electrostatic discharge currents** – using the same voltage divider BVR, the bearing voltage mirrors the CM voltage. During the capacitive bearing behavior, the electrically charged lubrication film, between the balls and the running surface, may break down when the bearing voltage exceeds a certain threshold. Thus, an Electric Discharge Machine

(EDM) current with high amplitude occurs [16]. Usually, the breakdown voltage of the lubricant is influenced by factors like metallic particles due to wear in the grease or operating temperature. Repetition of such EDM currents leads eventually to bearing damage;

**c) circulating bearing currents** – determined by the high voltage slope  $dV/dt$  at motor terminals, the CM ground current excites a circular magnetic flux around the motor shaft, thus inducing a shaft voltage. If this shaft voltage is high enough to puncture the lubricating film in the bearing, a circulating current occurs in the loop “stator – drive-end bearing – motor shaft – non drive-end bearing”. Thus, the bearing currents will have opposite direction in both bearings (differential mode) and will reflect the CM ground current;

**d) rotor ground currents** – this bearing current type occurs when the motor is connected to the ground through the load. Depending on the HF ground impedance of the stator housing and rotor, this current may reach high values and damage both motor and load bearings.

In conclusion, the CM voltage and the ground current (both directly related to  $dV/dt$  slope at the motor terminals) are the main causes for additional bearing currents in inverter-operated motor through long cables. Thus, accurate simulation models for the entire system are also required here, to study the effects and the mitigation techniques of these parasitic phenomena.

## 1.2 Simulation models for high-frequency domain

The “off-line” methods are very useful to study the parasitic effects in electric drives with long cables, as they considerably reduce the analysis time when compared to the classical methods on a real setup. Therefore, HF simulation models for electric drives have to be developed to reproduce the parasitic effects in frequency ranges between 50 kHz up to several MHz. In this work, the three components of an electric drive, i.e. inverter, cable and motor, are first analyzed separately and finally are combined together in a single simulation model, valid for the entire electric drive. The simulations are then compared to the measurements at a real-setup for validation of the model.

First, the inverter model was neglected in literature in most of the cases and replaced by a voltage source with a ramp function. In order to investigate the effect of the semiconductor devices and the mitigation techniques for parasitic phenomena (related to inverter control) a detailed HF model for inverter needs to be used. The starting point for such approach is the accurate modeling of the semiconductor devices, in this case the IGBT. Two major approaches can be identified in literature:

- the physics-based IGBT models are accurate but physical data like the dimensions of the individual layers, the doping profiles/concentrations or the charge carriers life time are not easily available from manufacturers [23] [24] (a thorough classification of the simulation models is offered in [28]);
- the behavior-based IGBT models are simpler than the first ones and reflect the IGBT behavior at the terminals using an equivalent circuit. The parameterization of the circuit elements is based on the physical phenomena inside the semiconductor layers, device measurements and information from data sheets [25] [26]. Therefore, simple parameterization methods can be easily applied for any type of IGBT module with less information needed.

In this work, the IGBT model from [26] is adopted and the parameterization methods detailed in subchapter 2.1. An additional improvement of the IGBT simulation model is proposed in section 3.2.1 to integrate the effects of the IGBT diffusion capacitance (slower turn-off transients) and diffusion capacitance of the anti-parallel diode (effect of reverse-recovery current).

Second, cable simulation models are necessary to investigate the wave propagation and estimate the cable impedance. Two approaches were identified also in this case:

- the transmission-line models rely on the transfer function of the cable, dependent on both time and space between the two ends (time after an inverter voltage pulse was sent through the cable and spread along the cable length). Although such approach is simple to implement and leads to small simulation times, it reproduces the cable losses only with the help of the damping constant. The coupling between phases cannot be modeled [29];
- the lumped-parameter models are based on distributed parameters building the elementary  $\Gamma$  section (equivalent circuit). Connecting a finite number of such sections in a ladder circuit, the traveling wave is simulated by successive loading and discharging processes of the components from each section. Such models are complex and the physical parameters needed (these are easy to obtain from data sheets), but lead to accurate results [31] - [33].

In subchapter 2.2, both approaches are investigated. However, the second approach is chosen and the parameterization methods are analyzed and developed. Because the model from [31] is strongly simplified and in [32] the losses are not properly represented, improvements for representing the cable losses (mainly generated by skin and proximity effects of the conductors at HF) are studied in section 3.2.2.

The motor represents the third main component of an electric drive. Therefore motor simulation models have been also investigated for more reasons: estimation of input impedance (to reproduce the reflection coefficient at the motor terminals), capacitive couplings between stator windings and between the stator winding and the stator iron (to simulate the nonlinear voltage distribution between the first winding coils and the CM ground current, respectively):

- the distributed-parameter motor models are based on traveling wave theory and similar to lumped-parameter models of the cable. More  $\Gamma$  sections build the entire model, the usually number of sections being equal to the number of turns. Such models are complex and the physical motor dimensions must be known for parameterization (exact number of turns per slot, slot dimension, etc.). Using the capacitive coupling between each turn ( $\Gamma$  section) the nonlinear voltage distribution can be reproduced [34];
- the behavior-based motor models are simpler than the previous ones, describing the behavior at the motor terminals using an equivalent circuit for each stator phase (considering only the stator winding is sufficient in studying the HF effects) [36]. The components of the equivalent circuit are derived by measurements of the input impedance at motor. Although they are easy to implement, these models do not deliver accurate results like distributed-parameter models (e.g. no simulation of nonlinear voltage distribution at first stator windings). Therefore, additional modifications are necessary, especially if the simulation of the bearing currents is required [35].

Because this work does not concentrate on the parasitic effects of the motor, but on those of the inverter and the cable, the second approach is found more appropriate due to simple parameterization methods required (detailed further in subchapter 2.3 together with the simulation model) and, like in the IGBT case, due to inaccessible physical dimensions of the motors. Simulation results are compared in section 3.2.3.

At the end, all individual models of the electric drive are connected together in a single simulation model. The results are presented in chapter 3 and further in chapter 4, where the mitigation techniques for HF parasitic effects are investigated.

### 1.3 Methods for reduction of parasitic effects

Since HF parasitic effects have been reported for the first time at electric drives with long feeders, many solutions for their reduction have been investigated in literature, regarding: improved modulation technique for CM voltage reduction [20], use of inverter output filters or cable terminators to decrease the voltage gradient and match the cable impedance, respectively [31] [37] and [38], improved insulation of the stator winding or isolated bearings [13], etc. In order to prove the efficiency of the “off-line” analysis method, using the simulation models, mitigation techniques from two main categories are discussed and compared in the final part of present work:

- *inverter-related* mitigation methods related to the inverter control. As the IGBT itself represents the source of steep voltages, it is possible to modify the switching characteristic of the IGBT. In subchapter 4.1 and 4.2 the following solutions are investigated: decreased voltage gradient at the inverter output using different gate resistances or active gate control [24], “2-step” voltage gradient using active gate control or three-level inverter topology [39], pre- and post-charge of cable stray elements [10];
- *cable-related* mitigation methods, presented in subchapter 4.3 and 4.4. They use additional circuits to match the cable impedance (cable terminators at the motor input) or to reduce the gradient of the voltage at the inverter output (inverter output filters);
- *quasi-resonant (QR) DC-link converter* used in electric drives with long cables [68]. This converter topology is thoroughly investigated together with the two main characteristics (motor friendliness and high energy efficiency) in chapter 5. Simulations are validated with measurements on a real setup.

For all above-mentioned methods, the simulations are used for the method implementation (filter design) and finally for evaluations. Measurements at a real setup are validating the simulation results, showing good agreement. A general overview for all evaluations, together with the general conclusions, is offered in chapter 6.

At the end, several measurements and parameter lists, used for parameterization of the simulation models, are collected in Appendix (chapter 7) for different cable types and motors.

## 2 High-frequency simulation models for electric drives

For investigations and development of reduction methods for HF parasitic effects in electric drives, reliable simulation models have to be analyzed. In this chapter, the electric drive is first treated separately considering the three main components: inverter, cable and motor. Then, all components are combined into a single simulation model. Thus, investigations are possible considering the entire system.

There are several approaches in modeling each electric drive component. On one hand, the physics-based model for IGBTs from [23] offers a good description of the switching dynamic, but it is complex and difficult to parameterize. A behavioral model, on the other hand, is easy to parameterize it since the IGBT is modeled using an equivalent circuit and the parameters are easily obtained from data sheets and direct measurements at the pins of the device [27]. Second, the cable models in the frequency-domain from [29] are fast, but they describe the cable only as a transmission system. The internal phenomena like capacitive coupling between phases and shield together with the asymmetries for different cable topologies are neglected in this case. A more complete model, without increasing the simulation burden too much, is offered by the lumped-parameter models [32]. Third, the electric motor can be modeled in HF range also with lumped-parameter circuits but, in this case, the geometry and the stator insulation properties must be known [34]. A simplified behavior model represents a good alternative [36].

Finally, by implementing all three time-domain simulation models in the circuit simulation software, they can be easily connected together and analyzed as a whole system. The Simplorer<sup>®</sup> simulation software provides a good solution for circuit-based models and time-domain simulations. All three single models are easily interconnected and simulated as a single circuit. Simplorer<sup>®</sup> offers also a high diversity of additional elements besides circuit elements: state machines, control blocks, equation blocks, etc. The user-friendly interface makes this simulation software easy to implement.

### 2.1 Inverter simulation model

As already mentioned, the inverters are using switching semiconductors to transfer the energy from DC link to motor or the other way around when the drive is braking. Using the pulse width modulation algorithm (PWM), a voltage of variable fundamental amplitude and frequency is obtained as mean values per pulse period. Thus, the line-to-line voltage at the inverter output jumps between 0 and DC-link voltage  $V_{DC}$  or between 0 and  $-V_{DC}$ . To model the HF behavior of these voltage pulses, the semiconductor model has to be considered.

The IGBT is used today at a large scale in industrial ASD. It represents the good combination between the bipolar junction transistor (BJT) and the MOSFET, by inheriting the favorable properties from both. Thus, the IGBT structure can block relative high voltage and show low on-state voltage due to the BJT structure. Furthermore, the IGBT is easy to control via the MOSFET gate structure, allowing the development of simple gate drive circuits. In this way, with low gate power required (high peak gate currents needed only at turn-on and turn-off transients), a high-power device can be controlled. Based upon these characteristics, the IGBT has been extensively used in applications exceeding 300V as an alternative to GTOs, BJTs and power MOSFETs [5] [40].

#### 2.1.1 IGBT semiconductor

##### 2.1.1.1 Semiconductor structure

The power IGBT has a vertical sandwich structure as shown in Figure 2.1, which is similar to that of a power MOSFET, except for a  $p^+$  layer at the bottom. More exactly, a planar cell of a Non Punch Through (NPT) is represented. The different types of IGBTs will

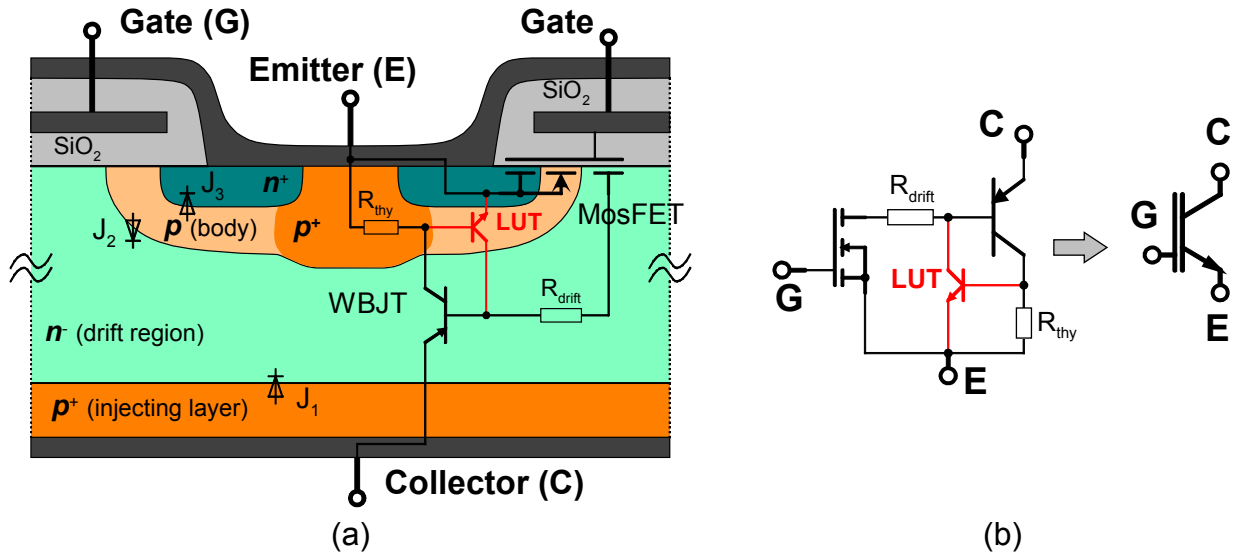


Figure 2.1: Cross-section (a) and equivalent schematic of an IGBT cell (b)

be detailed in next subsection. Figure 2.1 (b) represents the equivalent circuit of the IGBT cell and the graphic symbol.

The main IGBT components may be distinguished [40] [41]:

a) The MOSFET structure, represented by the high doped  $n^+$ -layer (source region), the  $p$ -layer (body region) and the low doped  $n^-$ -layer (drain) also called drift region. The electron channel is built up in the body region when the threshold voltage  $V_{th}$  is exceeded between gate and emitter metalization;

b) The Wide-Base Bipolar Junction Transistor (WBJT) has a  $pnp$  structure which is established between  $p$  body layer (collector region),  $n^-$  drift region (wide base) and highly doped injecting  $p^+$ -layer (emitter region). The base current of the BJT is supplied by the MOSFET part. The rest of the current flows from emitter to collector, contributing to the entire IGBT current. The wide area of the BJT determines low values of the BJT gain. Usually the current sharing between the two transistors is:  $I_{FET} > 60\%$  and  $I_{PNP} < 40\%$ ;

c) Third, the parasitic  $npn$  transistor (latch-up transistor LUT) is built by  $n^-$  drift region,  $p$  body layer and  $n^+$  source layer. Combined with the WBJT, it forms a thyristor that once turned on it cannot be turned off externally, unless the current is reduced to zero. In other words, a conduction path that avoids the MOS channel will be built. This may lead to destruction of the device. The main cause for the thyristor turn-on is the voltage at  $R_{thy}$ . To reduce this voltage following measures are taken: current through the WBJT is reduced; an additional doping in the body layer leads to smaller value of  $R_{thy}$ , see Figure 2.1 (a).

In Figure 2.1 (a) the junction diodes are also represented.  $J_2$  is responsible for taking the forward blocking voltage during the turn-off state, when the gate-emitter voltage is 0 or negative ( $J_2$  is reverse-biased for positive collector-emitter voltage  $V_{CE}$ ). The diode  $J_1$  is taking the reverse blocking voltage ( $J_1$  is reverse-biased for negative  $V_{CE}$ ). Comparing the two junctions, it can be noticed that  $J_2$  can support a large voltage due to the wide and poorly doped drift region. However,  $J_1$  supports lower breakdown voltages than  $J_2$  because the concentration of  $p^+$  collector-side layer is greater than of the  $p$ -body layer. It is well known that the breakdown voltage of  $pn$ -junctions, with different doping concentrations, decreases with higher doping level of the high-doped side [42]. The reverse breakdown voltage has, however, no major importance because in most of the cases, the IGBT is connected in anti-parallel with a freewheeling diode [2].

### 2.1.1.2 IGBT functionality

Because the IGBT is a combination between the FET and the BJT, it allows a bipolar current flow. In Figure 2.2 (a) the flow of the carriers inside the IGBT structure is shown.

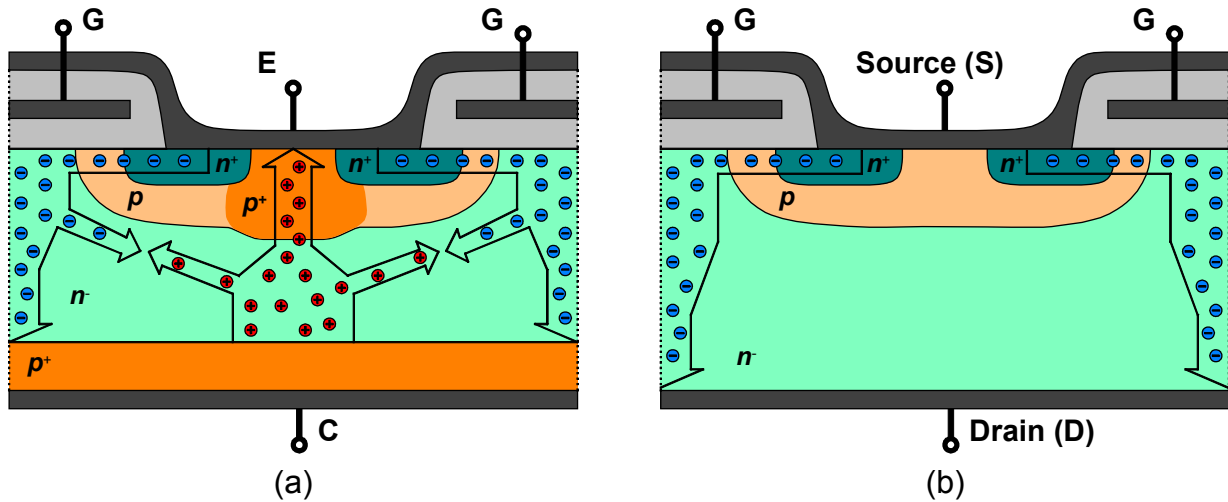


Figure 2.2: IGBT current flow (a) and MosFET current flow (b)

The majority carriers will flow from the emitter side  $n^+$  layer through the FET channel into the drift region as soon as the channel is built. Once they reach the edge of junction  $J_1$ , holes will be injected from collector side  $p^+$  layer into drift region and flowing further to body layer and emitter. Thus, a bipolar current occurs, making the voltage drop  $V_{CE}$  during conduction small. However, at the MOSFET only the majority carriers form the current as no injecting layer exists. Hence, the drain-source voltage drop  $V_{DS}$  during conduction is bigger (see Figure 2.2 (b)) causing more conduction losses. Yet, the unipolar structure of the FET allows a higher switching dynamic because the current is built only from electrons.

In Figure 2.3 the output characteristics for IGBT and MOSFET are presented. When the MOSFET is turned-on, i.e. is in the linear region, the relation between the drain current  $I_D$  and the drain-source voltage  $V_{DS}$  is nearly linear indicating a resistive behavior. In the saturation region (seen from the physic point of view) the carrier flow starts to saturate although the voltage  $V_{DS}$  is increased further (pinch-off effect of the MOS channel). Because both positive and negative carriers contribute to the current flow at the IGBT, the behavior in the saturation region (seen from the power electronic point of view) is that of a diode and indicates a minimum voltage drop  $V_{CE}$  for a given collector current  $I_C$ . The current increases exponentially with voltage, resulting in a lower voltage drop in the saturation region. Moreover, the  $p^+$  substrate is missing at the MOSFET. When a negative bias voltage  $V_{DS}$  is applied, the device is conducting due to the  $pn$  junction between the body layer and the drift region. This junction is also called internal body diode. The additional  $p^+$ -layer in the IGBT prevents the reverse conduction. Therefore, an anti-parallel diode must be connected externally to the IGBT chip in VSI applications.

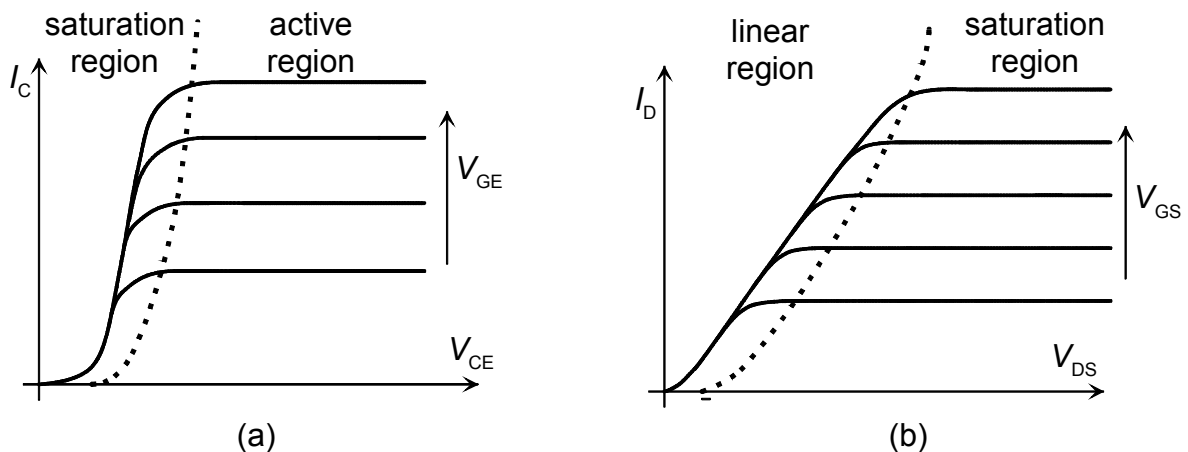


Figure 2.3: Static output characteristics for IGBT (a) and MOSFET (b)

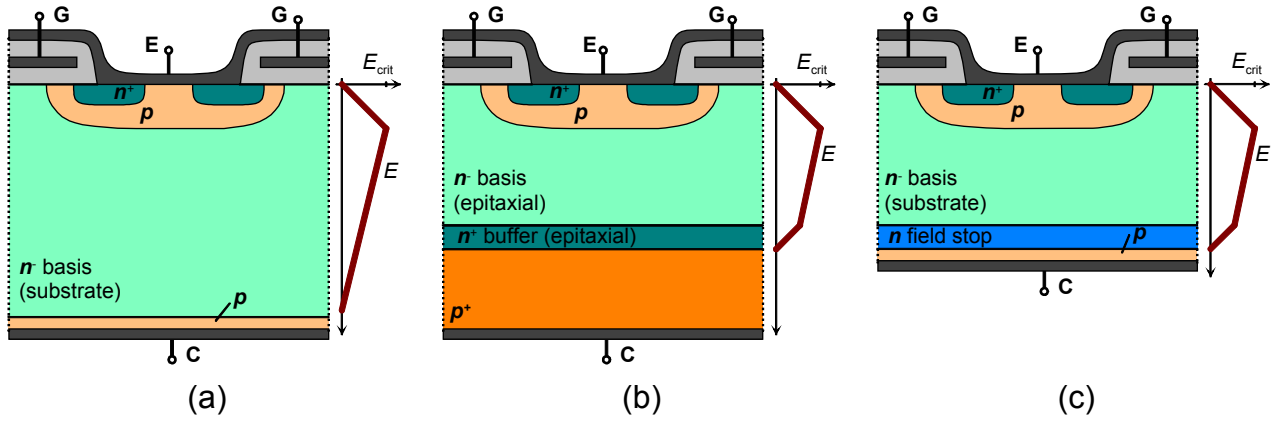


Figure 2.4: IGBT topologies regarding the vertical structure: (a) NPT, (b) PT and (c) FS IGBT.

### 2.1.1.3 Types of IGBT devices

Regarding the internal structure from Figure 2.1 (a), different types of IGBT can be found on the market, each with advantages and disadvantages.

A first classification considers the vertical structure:

- the non-punch-through (NPT) IGBT has a wide drift region, see Figure 2.4 (a), to accommodate the electric field  $E$ . The field is not allowed to reach the  $p^+$  collector side and its intensity profile is always triangular. The maximum field strength occurs at the upper  $pn$  junction, as shown in the right figure, and should not exceed the critical value  $E_{crit}$ . Because the breakdown voltage is proportional to the area underneath the field curve, a high voltage may be blocked only with a thick drift region. However, thicker drift region results in higher drift resistance and hence higher saturation voltage. While the  $E$  field expands in the drift region during turn-off transient, some carriers remain outside until they are swept out or recombine. Long carrier lifetime, due to the low-doped shallow collector region, leads to long and low-amplitude tail currents [25];

- in the punch-through (PT) or asymmetrical IGBT, presented in Figure 2.4 (b), a heavily-doped  $n^+$  buffer layer is inserted between the  $p^+$  injection layer and the  $n^-$  drift region. Thus, the injection efficiency of the  $p^+$  substrate is improved and the minority carrier lifetime in the drift region is reduced. Thus, the tail currents are eliminated. The electric field is allowed to reach the buffer layer, having a trapezoidal profile in this case. A thinner drift region determines also a lower on-state voltage drop. One disadvantage of PT topology is the higher switching losses due to the higher carrier concentration in the  $n^+$  buffer layer. High injection level of the minority carriers requires lifetime control, which determines a negative temperature coefficient for on-state resistance. Thus, paralleling of

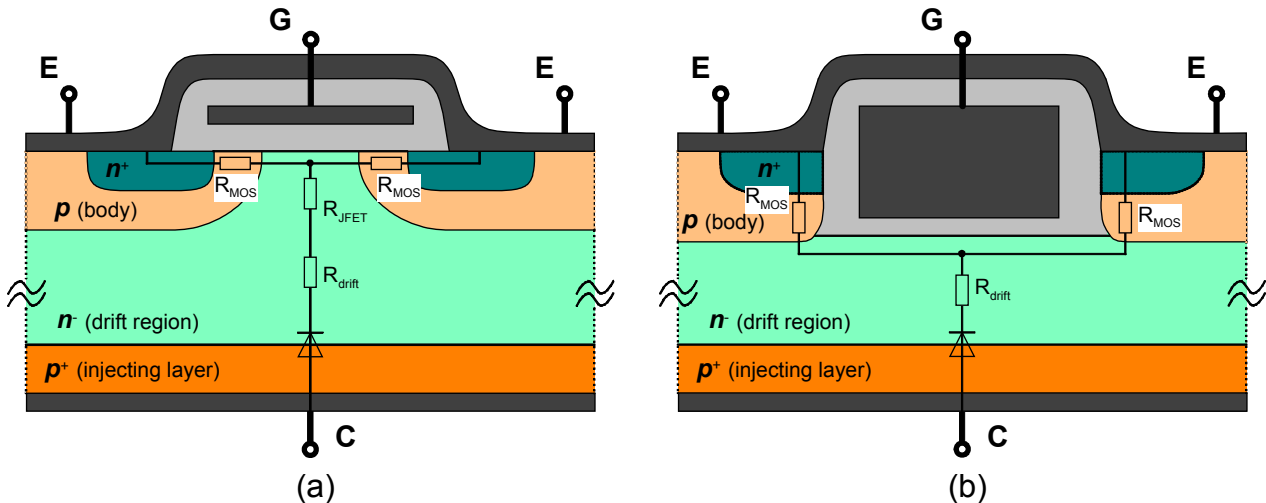


Figure 2.5: IGBT topologies regarding the MOS cell layout: (a) planar and (b) trench IGBT



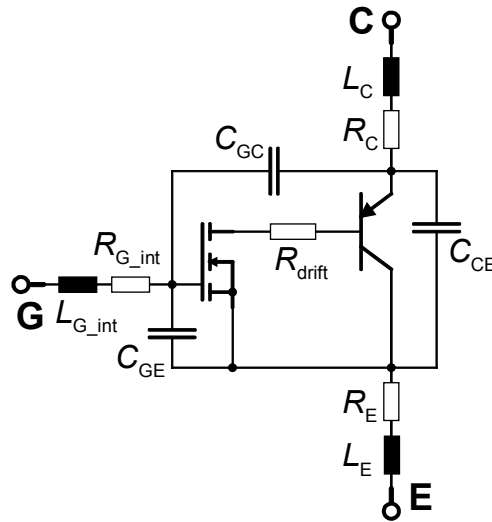


Figure 2.6: IGBT equivalent circuit with stray elements

single chips is more difficult than in NPT case (positive temperature coefficient) [25];

➤ Figure 2.4 (c) shows the field-stop (FS) or soft-punch-through (SPT) design, which represents the combination between the previous two topologies and inherits the advantages from both. The drift region is thin and determines a small voltage during the on state. Moreover, a buffer layer is used to stop the electric field. Like for NPT topology, the electric field has a trapezoidal shape. Also a shallow collector region is used to obtain a low injection level for minority carrier and therefore, positive temperature coefficients [25].

A second classification is obtained by considering the MOS cell:

➤ the planar IGBT (Figure 2.5 (a)), which was presented until now, has an horizontal layout of the MOS cell;

➤ on the contrary, the trench IGBT (Figure 2.5 (b)) presents a vertical structure of the MOS cell using a buried gate metalization deep into the drift region. Thus,  $R_{JFET}$  is avoided, resulting in a lower on-state voltage. The vertical layout of the MOS channel allows a higher current density and increases the latch-up immunity. However, there are also disadvantages like increased gate capacitances, leading further to poor dynamic properties or higher gate currents from gate driver units.

#### 2.1.1.4 Parasitic elements

Like any other real devices, the IGBTs possess stray elements. Considering the equivalent circuit from Figure 2.1 (b), the **npn** latch-up transistor (LUT) can be neglected in a good design together with  $R_{thy}$ . Adding the stray elements, the equivalent circuit is shown in Figure 2.6.

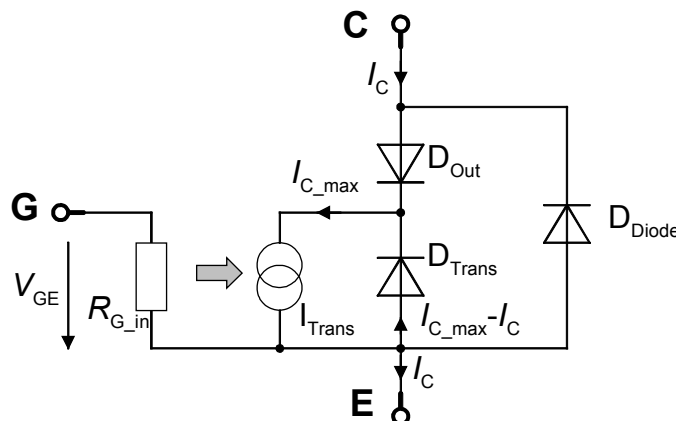


Figure 2.7: IGBT equivalent circuit for steady-state behavior

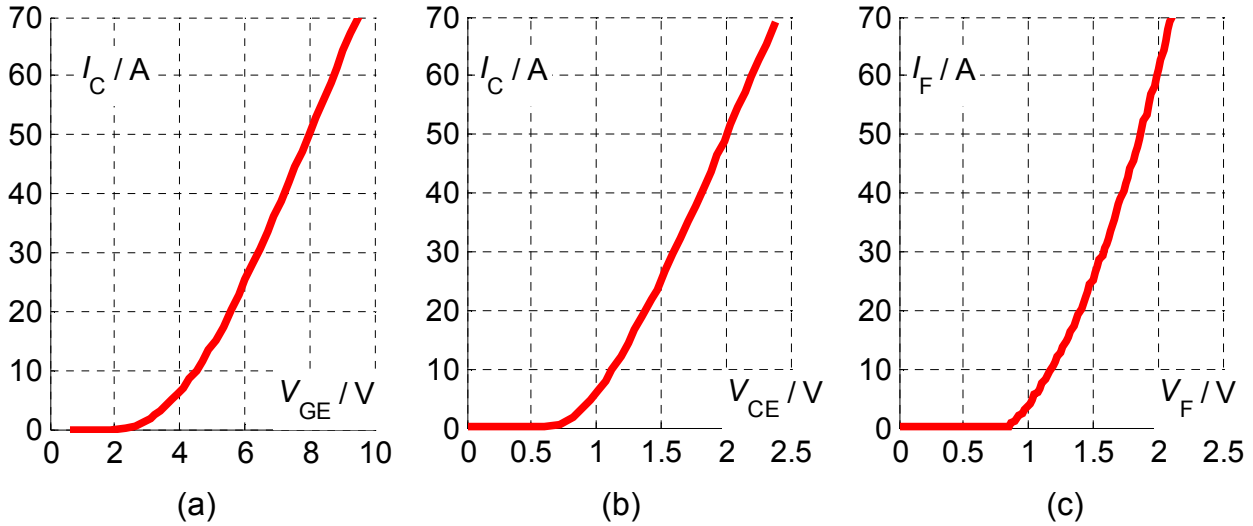


Figure 2.8: IGBT's transfer (a) and output characteristic (b); (c) Diode characteristic

- stray resistances and inductances of the bonding wires:  $R_{G\_int}$ ,  $L_{G\_int}$  for gate connection;  $R_E$  and  $L_E$  for emitter and  $R_C$  and  $L_C$  for collector connection.
- stray capacitances between the three connections: gate-emitter capacitance  $C_{GE}$ , gate-collector capacitance  $C_{GC}$  and collector-emitter capacitance  $C_{CE}$ .

Here,  $C_{GE}$  and  $C_{GC}$  are of great importance as they have a great influence on the gradients of the collector current  $dI_C/dt$  and collector-emitter voltage  $dV_{CE}/dt$  [27].

## 2.1.2 IGBT behavioral model

In literature, there are two major approaches to model the IGBT semiconductor device: *physics-based* and *behavioral* description.

The first type of models have a high accuracy, but they are complex and based mostly on physical semiconductor parameters: doping concentration of each layer, width of  $n^-$  drift region, used materials, etc. Normally, the semiconductor manufacturer does not publish this data, which makes the parameterization impossible.

The second approach is adopted here because the IGBT behavioral description is easy to implement from data-sheet parameters and individual measurements at the IGBT module. For exemplification, a field-stop, trench IGBT from Infineon® (6-pack module FS35R12YT3) was chosen to build the model [43].

### 2.1.2.1 Description of the steady-state behavior

The IGBT steady-state model is based on the equivalent circuit from Figure 2.7, where the circuit components are derived from the IGBT structure.

First, the transfer characteristic describes the relation between the applied gate-emitter voltage  $V_{GE}$  and the collector current  $I_C$ , namely the  $I_C = f(V_{GE})$  relation (graphic) from data sheet, see Figure 2.8 (a). This is represented by a voltage-controlled current source  $I_{Trans}$ . The input gate impedance is high due to the MOS structure and is represented by a very large resistance  $R_{G\_in}$ . Thus, the steady-state gate current can be neglected.

In VSIs, a turned-on IGBT is operated always in the saturation region and  $V_{GE}$  has its nominal value. From the transfer characteristic, a single value for  $I_C$  corresponds to a single value of  $V_{GE}$  and junction temperature, resulting in a single point of operation. But the collector current depends also on the rest of the circuit to which the IGBT is connected. To reflect this flexibility, an ideal freewheel diode  $D_{Trans}$  is connected in parallel to the current source  $I_{Trans}$ . Thus, for a given voltage  $V_{GE}$ , a maximum current value  $I_{C\_max}$  will correspond. The difference between  $I_{C\_max}$  and  $I_C$  will flow through the diode  $D_{Trans}$ . Next, the voltage drop  $V_{CE}$  during conduction is given by the output characteristic  $V_{CE} = f(I_C)$ .



### 2.1.2.3 Parameter identification

For steady-state behavior, the main characteristics are taken from the data sheet [43] and shown in Figure 2.8. The Simplorer® simulation software offers a tool to scan the characteristics from data sheets and to store the curves as data pairs. The values between the data pairs are linearly interpolated. Therefore, a good resolution (many data pairs) is desired. To avoid unexpected errors, e.g. infinite saturation voltages for undefined current values, it is strongly recommended to extend the depicted domain by an extrapolation [25].

As already mentioned, the dynamic behavior is influenced mainly by capacitances and bond-wire inductances. In Figure 2.9 (b) the distributed capacitances inside the semiconductor structure are presented. First, the capacitance  $C_{GE}$  results from a parallel connection between the gate-source capacitance of the internal MOSFET ( $C_{GS}$ ) and the oxide capacitance ( $C_M$ ). While the latter is fixed and depends on the module construction,  $C_{GS}$  is voltage dependent. For negative  $V_{GE}$ , additional accumulation of holes in the p-body layer underneath the gate electrode, phenomena also known as accumulation process, determines a higher value for  $C_{GS}$ . When  $V_{GE}$  is low or positive, the holes are no longer accumulated in this region and  $C_{GS}$  has lower values (for  $V_{GE} > V_{GE\_th}$  body layer is swamped with electrons under the gate metalization and the channel is built) [26].

Second, the capacitance  $C_{GC}$  is responsible for the  $V_{CE}$  gradient and it is formed by a series connection of three capacitances:  $C_{OX}$ ,  $C_{Depl.}$  and  $C_{BE}$ . The oxide capacitance  $C_{OX}$ , like  $C_M$ , is fixed and depends on the module construction. The base-emitter capacitance  $C_{BE}$  is formed by a parallel connection between the diffusion capacitance at the collector-side **pn** junction ( $J_1$ ), when IGBT is forward biased, and the  $J_1$  junction capacitance for negative  $V_{CE}$ . On one hand, the diffusion capacitance can be neglected during switching transients and on the other hand, the IGBT is not used with negative blocking voltages in most of the cases, making this collector-side **pn** junction capacitance neglectable [42].

The capacitance  $C_{Depl.}$  varies with the applied gate-collector voltage  $V_{GC}$ . When  $V_{GC}$  is negative a carrier-depleted region inside the drift region, i.e. Space Charge Region (SCR), is present and acts like a dielectric, building the capacitance  $C_{Depl.}$ . As the width of the SCR changes with the applied voltage so does the capacitance value  $C_{Depl.}$  also. In Eq. 2.1 the relation between the width  $w_j$  of SCR and the  $C_{Depl.}$  value is given:

$$C_{Depl.} = \frac{\epsilon_{Si} A_{Depl.}}{w_j} \quad \text{Eq. 2.1}$$

with

$$w_j = \sqrt{\frac{2\epsilon_{Si}(V_D - V_{GC})}{e \cdot N_D}}, \quad \text{Eq. 2.2}$$

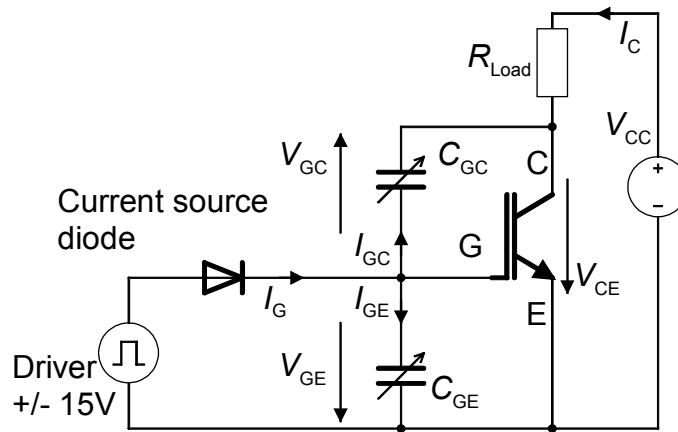
where  $A_{Depl.}$  is the surface of carrier-depleted region,  $\epsilon_{Si}$  represents electrical permittivity of the drift-layer,  $e$  stands for electron charge,  $N_D$  is donor concentration and  $V_D$  stands for diffusion potential.

Inserting Eq. 2.2 in Eq. 2.1, the voltage dependence  $C_{Depl.} = f(V_{GC})$  is obtained:

$$C_{Depl.} = \frac{A_{Depl.} \cdot \sqrt{\epsilon_{Si} \cdot e \cdot N_D}}{\sqrt{2(V_D - V_{GC})}} = \frac{C_0}{\sqrt{1 - \frac{V_{GC}}{V_D}}}, \quad C_0 = \frac{A_{Depl.} \cdot \sqrt{\epsilon_{Si} \cdot e \cdot N_D}}{\sqrt{2V_D}} = \text{const.} \quad \text{Eq. 2.3}$$

Here,  $C_0$  represents the capacitance value at  $V_{GC} = 0$ . Considering the series connection of  $C_{Depl.}$  and  $C_{OX}$ , following values for  $C_{GC}$  can be determined:

$$C_{GC} = \begin{cases} \approx C_{Depl.}, & \text{for } V_{GC} \ll 0 \\ \frac{C_{Depl.} \cdot C_{OX}}{C_{Depl.} + C_{OX}}, & \text{for } V_{GC} \geq 0 \end{cases} \quad \text{Eq. 2.4}$$



**Figure 2.10: Measurement setup for input capacitance determination**

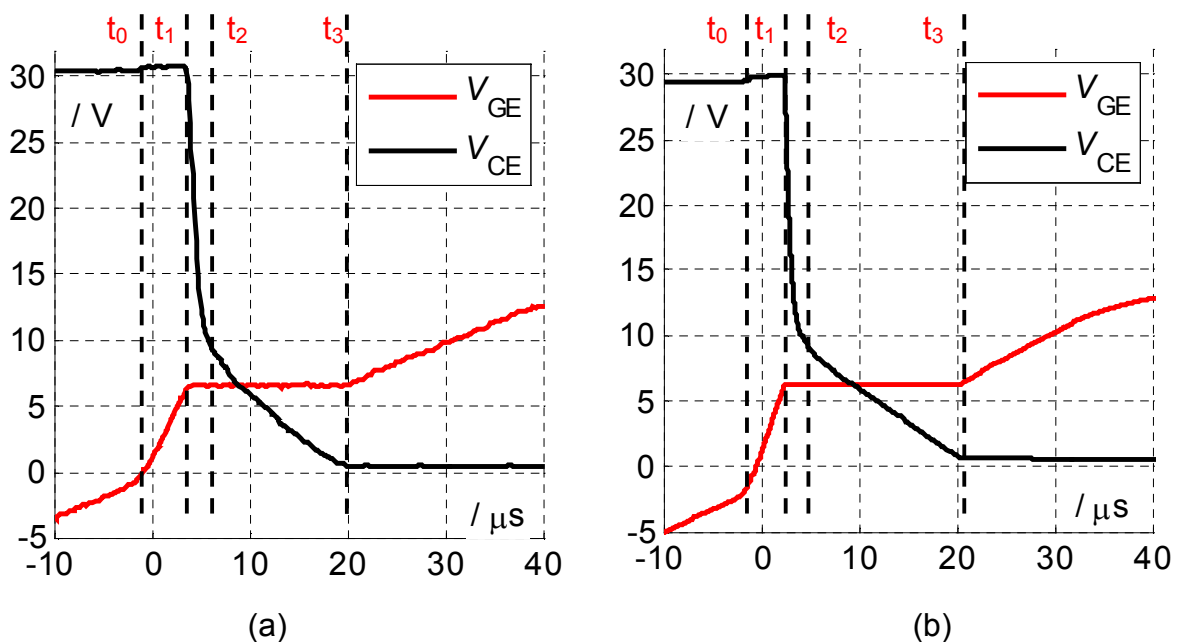
In other words, when  $V_{GC}$  has large negative values the SCR capacitance  $C_{Depl.}$  is very small (1 to 2 orders of magnitude smaller than  $C_{OX}$  due to larger width) and it will be dominant. As  $V_{GC}$  approaches to zero,  $w_j$  decays and  $C_{Depl.}$  increases. For  $V_{GC} > 0$ , the capacitance  $C_{Depl.}$  becomes large and the effect of the constant capacitance  $C_{OX}$  cannot be neglected anymore.

To determine the IGBT **input capacitance**  $C_{ies}$ , formed by  $C_{GE}$  and  $C_{GC}$ , the measurement setup from Figure 2.10 is used. A constant current source, implemented by a constant current diode, loads the input capacitance. The current should be small due to the small capacitance values and to avoid the effect of the eventually stray inductances. A high resistive load  $R_{Load}$  is used to avoid high collector currents.

Figure 2.11 shows the measured and simulated waveforms for  $V_{GE}$  and  $V_{CE}$  during the IGBT turn-on transient, using a constant gate current of  $I_G = 3.6$  mA. For constant  $I_G$ , the Eq. 2.5 is valid [25]:

$$I_G = C_{GC} \cdot \frac{dV_{GC}}{dt} + C_{GE} \cdot \frac{dV_{GE}}{dt} + \frac{dC_{GC}}{dV_{GC}} \cdot \frac{dV_{GC}}{dt} \cdot V_{GC} + \frac{dC_{GE}}{dV_{GE}} \cdot \frac{dV_{GE}}{dt} \cdot V_{GE} \quad \text{Eq. 2.5}$$

The first two terms represent the components of the gate current for voltage-time dependency, while the last two consider the capacity-voltage dependency. Following time intervals can be distinguished during the gate charging process:



**Figure 2.11: Measured (a) and simulated (b) gate charging characteristic for low blocking voltage**

**Interval 1:** time before  $t_0$ 

The constant gate current charges the effective capacitance  $C_{ies} = C_{GC\_min} + C_{GE\_max}$  and  $V_{CE}$  remains constant. Here,  $C_{GE}$  has its maximum value due to the accumulation of holes in the  $p$  body layer under the gate metalization.  $C_{GC}$  has its minimal value because the SCR width is maximal.  $V_{GC}$  can be calculated using the Kirchhoff 2<sup>nd</sup> law for IGBT:

$$V_{GC} = V_{GE} - V_{CE}. \quad \text{Eq. 2.6}$$

Applying a derivative to Eq. 2.6 we get:

$$\frac{dV_{GC}}{dt} = \frac{dV_{GE}}{dt} - \frac{dV_{CE}}{dt}, \quad \text{Eq. 2.7}$$

and having  $V_{CE}$  constant, an important relation for this time interval is obtained:

$$\frac{dV_{GC}}{dt} = \frac{dV_{GE}}{dt}. \quad \text{Eq. 2.8}$$

Inserting Eq. 2.8 in Eq. 2.5 and assuming constant capacitance values for this time interval, following relation is obtained:

$$I_G = (C_{GC\_min} + C_{GE\_max}) \frac{dV_{GE}(t < t_0)}{dt} = C_{ies\_max} \frac{dV_{GE}(t < t_0)}{dt}. \quad \text{Eq. 2.9}$$

From Figure 2.11, the voltage slope is  $dV_{CE}(t < t_0)/dt \approx 0.322 \text{ V}/\mu\text{s}$  and according to Eq. 2.9 the capacitance is  $C_{ies\_max} = 11.18 \text{ nF}$ .

**Interval 2:** time between  $t_0$  and  $t_1$ 

Here  $C_{GE}$  decreases to  $C_{GE\_min}$  because the carrier accumulation under gate metalization vanishes determining a change in voltage slope  $dV_{GE}/dt$ . From Figure 2.11 a small increase in  $V_{CE}$  is observed but this can be neglected and therefore considered as constant, making Eq. 2.8 valid also for this case. A different  $V_{GE}$  voltage slope is noticed:  $dV_{GE}(t = t_0)/dt \approx 1.662 \text{ V}/\mu\text{s}$ . Now Eq. 2.9 becomes:

$$I_G = (C_{GC\_min} + C_{GE\_min}) \frac{dV_{GE}(t = t_0)}{dt} = C_{ies\_min} \frac{dV_{GE}(t = t_1)}{dt}, \quad \text{Eq. 2.10}$$

and we obtain  $C_{ies\_min} = 2.16 \text{ nF}$ , which corresponds to the data sheet value [43]. There is no change in  $C_{GC}$  value because the width  $w_j$  of SCR remains unchanged.

**Interval 3:** time between  $t_1$  and  $t_2$ 

The Miller plateau is reached, i.e.  $dV_{GE}/dt = 0$ , and the constant gate current  $I_G$  charges only the capacitance  $C_{GC}$ . From Eq. 2.7 we get:

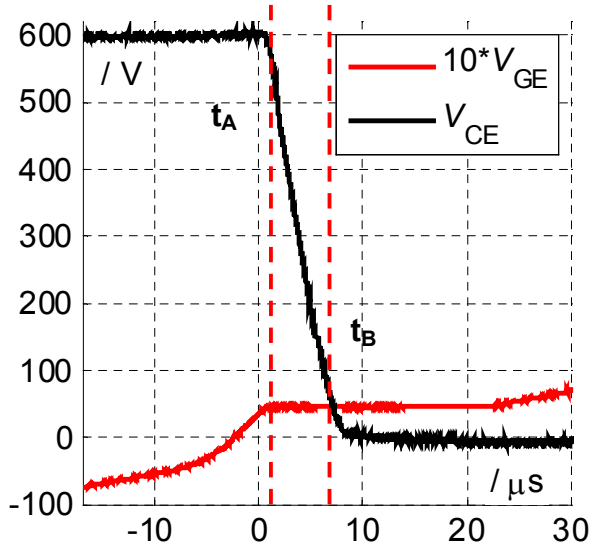
$$\frac{dV_{GC}}{dt} = - \frac{dV_{CE}}{dt}, \quad \text{Eq. 2.11}$$

and inserting Eq. 2.11 in Eq. 2.5, the minimal value for the gate collector capacitance  $C_{GC}$  is obtained:

$$C_{GC\_min}(V_{CE}=30 \text{ V}) = - \frac{I_G}{dV_{CE}(V_{CE}=30 \text{ V}) / dt} = \frac{3.6 \text{ mA}}{21.818 \text{ V}/\mu\text{s}} \approx 0.165 \text{ nF}.$$

To reflect the high-voltage effect on the SCR and further on the Miller capacitance  $C_{GC}$ , a similar test like in Figure 2.10 was conducted, but with a high  $V_{CC} = 600 \text{ V}$ . The load resistance  $R_{Load}$  has been recalculated to allow the same small  $I_C$  flowing from collector to emitter. The measurement is presented in Figure 2.12. The voltage  $V_{GE}$  is scaled with a factor 10 to obtain a good representation. By calculating the voltage slope  $dV_{CE}/dt$  and considering Eq. 2.11, the minimal value for the capacitance  $C_{GC}$  is obtained:

$$C_{GC\_min}(V_{CE}=600 \text{ V}) = - \frac{I_G}{dV_{CE}(V_{CE}=600 \text{ V}) / dt} = \frac{3.6 \text{ mA}}{81.25 \text{ V}/\mu\text{s}} \approx 44 \text{ pF}.$$



**Figure 2.12: Measured gate charging characteristic for high blocking voltage**

increases from its minimal to its maximal value, which is determined by the dominating oxide capacitance  $C_{OX}$ , according to Eq. 2.4. In Figure 2.11 it is noticeable that the inflection point in  $V_{GC}$  characteristic is situated not at 0V but earlier, see Figure 2.13 b). This point corresponds to the inflexion of  $C_{GC}$  characteristic and is located at:

$$V_{CGC} = V_{GE}(t_2) - V_{CE}(t_2) = 6.66 \text{ V} - 10.1 \text{ V} = -3.44 \text{ V}.$$

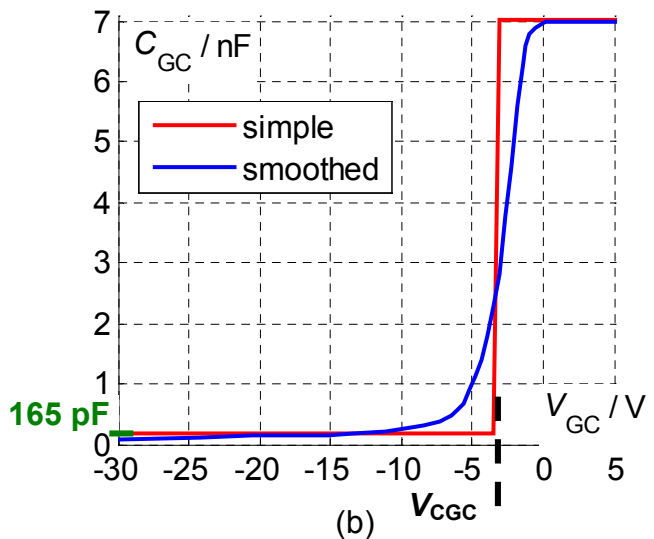
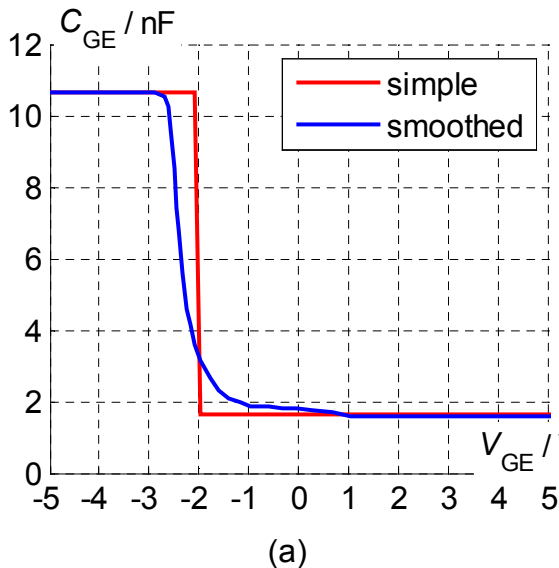
By inserting this voltage into  $C_{GC}$  characteristic, Eq. 2.4 becomes:

$$C_{GC} = \begin{cases} \approx C_{Depl.}, & \text{for } V_{GC} < V_{CGC} \\ \frac{C_{Depl.} \cdot C_{OX}}{C_{Depl.} + C_{OX}}, & \text{for } V_{GC} \geq V_{CGC} \end{cases} \quad \text{Eq. 2.12}$$

#### **Interval 5:** time after $t_3$

The Miller plateau is left and the gate current  $I_G$  charges further  $C_{GE}$  and  $C_{GC}$ . Now, the capacitance  $C_{ies}$  has following expression:

$$C_{ies} = C_{GE\_min} + C_{GC\_max}.$$



**Figure 2.13: Gate-Emitter capacitance (a) and gate-collector capacitance (b) characteristics**

This small value represents the extrapolation limit of the  $C_{GC}$  characteristic for high  $V_{CE}$ . For a better approximation of the depletion capacitance at high collector-emitter voltage  $V_{CE} = 600 \text{ V}$ , the measurement from Figure 2.12 will be used.

#### **Interval 4:** time between $t_2$ and $t_3$

$V_{CE}$  changes its slope while the gate charging is still in Miller-plateau phase ( $dV_{GE}/dt = 0$ ). Eq. 2.11 is valid here too and  $C_{GC}$  has the following expression:

$$C_{GC\_max} = -\frac{I_G}{dV_{CE}(t=t_2)/dt} = \frac{3.6 \text{ mA}}{0.5134 \text{ V}/\mu\text{s}} \approx 7.01 \text{ nF}.$$

In this time interval, the capacitance  $C_{GC}$

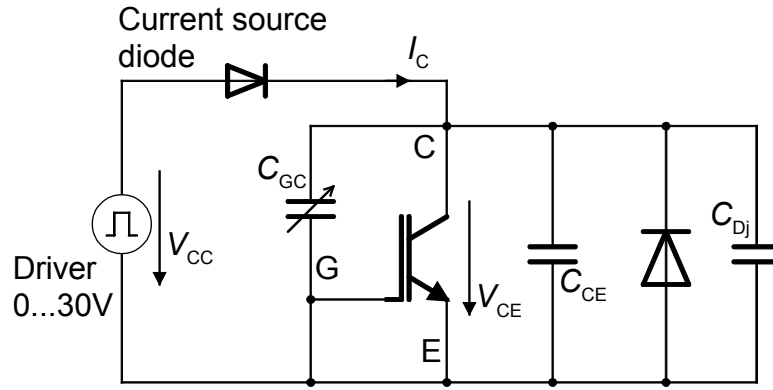


Figure 2.14: Measurement setup for output capacitance determination

The simple capacitance-voltage characteristics for  $C_{GE}$  and  $C_{GC}$ , determined from the individual time intervals mentioned before, are presented in Figure 2.13 with red lines. Because smoother characteristics lead to better simulation results, the following approximation is adopted: the capacitance derivative  $dC/dV$  is neglected during the intervals 1 and 2 for  $C_{GE}$  and 3 and 4 for  $C_{GC}$ , respectively. Thus, the Eq. 2.5 is strongly simplified and further used in Matlab® to calculate the smoothed characteristics during the transitions between these intervals; see the blue lines in Figure 2.13. Although the obtained results are not exact, the initial and the final value remain unchanged. The smoothed characteristics are further used in the IGBT simulation model.

The **collector-emitter capacitance**  $C_{CE}$  has a minor influence on the IGBT switching characteristic. However this can be determined using the measurement setup from Figure 2.14. A constant current diode is used here, too. Having the gate and emitter short-circuited, the IGBT is blocking and the output capacitance consists of a parallel connection between  $C_{GC}$ ,  $C_{CE}$  and diode junction capacitance  $C_{Dj}$ :

$$C_{oes} = C_{GC} + C_{CE} + C_{Dj}.$$

Eq. 2.13

The capacitance  $C_{GC}$  has been previously determined and can be included in Eq. 2.13. Because the diode cannot be separated from the IGBT chip,  $C_{CE}$  and  $C_{Dj}$  are set equal. For further simplification they are approximated by a constant value. In Figure 2.15 the simulated and measured curves for  $V_{CE}$  are shown. Two points are considered at  $t_1$  and  $t_2$ ,

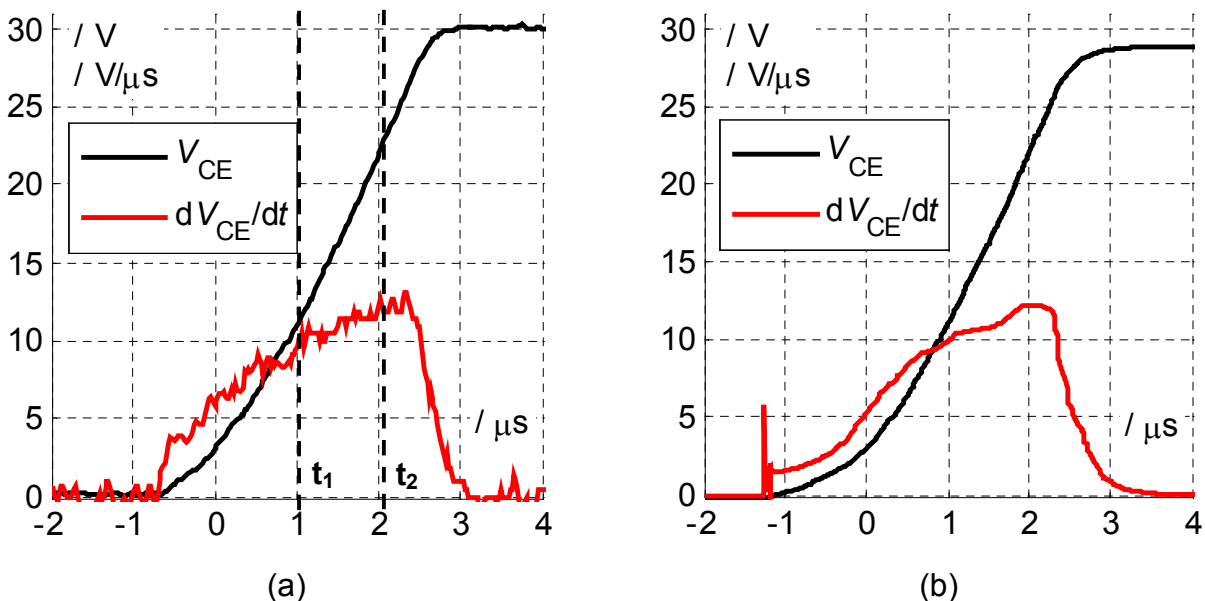


Figure 2.15: Measured (a) and simulated (b) output capacitance charging characteristic



Table 2.1: Calculation example for output capacitance

$t_1 = 1 \mu\text{s}$	$t_2 = 2 \mu\text{s}$
$V_{CE} = 22 \text{ V};$ $V_{GC} = -V_{CE} + V_{CGC} = -25.44 \text{ V};$ $\frac{dV_{CE}}{dt} \approx 12.18 \frac{\text{V}}{\mu\text{s}} \Rightarrow C_{oes}(t_1) \approx 267 \text{ pF};$ $C_{GC}(t_1) = 98 \text{ pF} \Rightarrow C_{CE} = C_{Dj} = 84.5 \text{ pF}.$	$V_{CE} = 11.1 \text{ V};$ $V_{GC} = -V_{CE} + V_{CGC} = -14.54 \text{ V};$ $\frac{dV_{CE}}{dt} \approx 10 \frac{\text{V}}{\mu\text{s}} \Rightarrow C_{oes}(t_2) \approx 325 \text{ pF};$ $C_{GC}(t_2) = 172 \text{ pF} \Rightarrow C_{CE} = C_{Dj} = 76.5 \text{ pF}.$

respectively. To determine the capacitance  $C_{oes}$ , Eq. 2.14 is used. By reading the value for  $C_{GC}$  capacitance from Figure 2.13 (b), the collector-emitter capacitance  $C_{CE}$  is calculated with Eq. 2.15. In Table 2.1 the calculations are detailed for  $t_1 = 1 \mu\text{s}$  and  $t_2 = 2 \mu\text{s}$ . A slight change in  $C_{CE}$  is observed whereas  $C_{GC}$  is changing app. 100% its value. Therefore, a constant value of 80 pF is adopted for  $C_{CE}$  and  $C_{Dj}$  in the IGBT simulation model. The simulation of the charge characteristic for the output capacitance is presented in Figure 2.15 (b). A good agreement can be observed between measurements and simulations.

$$C_{oes} = \frac{I_C}{dV_{CE}/dt}. \quad \text{Eq. 2.14}$$

$$C_{CE} = C_{Dj} = (C_{oes} - C_{GC})/2. \quad \text{Eq. 2.15}$$

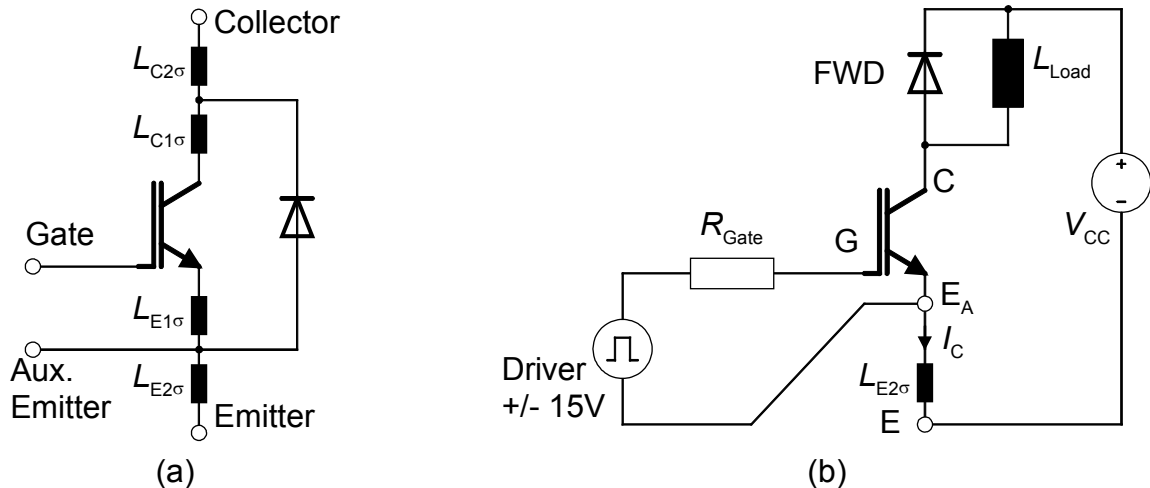
The maximum reachable voltage with this setup is  $V_{CC} = 30 \text{ V}$ . For higher voltages, the  $C_{CE}$  and  $C_{Dj}$  capacitance values are extrapolated with the already-mentioned value.

The values for the **Internal gate resistance** and the **bond-wire resistances** are to be found in the data sheet. For the chosen module they are:

$$R_{G\_int} = 6 \Omega,$$

$$R_{CC'+EE'(\text{switch})} = R_{CC'+EE'(\text{arm})}/2 = 2 \text{ m}\Omega.$$

Together with the bond-wire resistance, the total **stray inductance** for a single switch is given  $L_{TOT} = L_{\sigma CE} = 35 \text{ nH}$ . Figure 2.16 (a) shows the considered distribution of this stray inductance in the switch-diode connection. First, the dominating stray inductances  $L_{C2\sigma}$  and  $L_{E2\sigma}$  are between the module pins and the semiconductor chip. Because the anti-parallel diode cannot be separated, the stray inductances between this and the IGBT chip are also represented:  $L_{C1\sigma}$  and  $L_{E1\sigma}$ . The last one is important because it influences the slope  $dI_C/dt$  of the collector current.

Figure 2.16: Stray inductance distribution (a) and  $L_{E2\sigma}$  measurement setup (b)

To determine the total stray inductance, the measurement setup from Figure 2.16 (b) is used. Here, the stray inductance  $L_{E2\sigma}$ , between auxiliary ( $E_A$ ) and main emitter connection ( $E$ ), is calculated from the measured voltage drop when a constant slope is applied to the collector current. This is realized using a buck converter topology and applying a short pulse to the gate. A low inductive load is used to get a high rise for  $I_C$  and therefore, a reasonable voltage drop on the small  $L_{E2\sigma}$ . During the measurement, a rise in  $I_C$  from 0 to 28.7 A in 30.2  $\mu\text{s}$  was obtained. The gradient  $dI_C/dt = 0.95 \text{ A}/\mu\text{s}$  produces a voltage drop on  $L_{E2\sigma}$  of app.  $U_{EA\_E} = 14.1 \text{ mV}$ . Using Eq. 2.16, the stray inductance is calculated.

$$L_{E2\sigma} = \frac{V_{EA\_E}}{dI_C/dt} \approx 14.9 \text{ nH}. \quad \text{Eq. 2.16}$$

Further, a symmetrical construction is assumed, i.e. the connection between chip and collector has the same length as the one between chip and emitter. Thus, it can be considered that they have the same inductance  $L_{E2\sigma} = L_{C2\sigma}$ .  $L_{E1\sigma}$  and  $L_{C1\sigma}$  cannot be determined separately without cutting the physical connection between the IGBT chip and the anti-parallel diode. That is why, the individual stray inductances are grouped into  $L_{CE1}$  and  $L_{CE2}$ , like Figure 2.9 (a) shows. The values for both inductances are estimated to be:

$$L_{CE1} = L_{E2\sigma} + L_{C2\sigma} = 29.8 \text{ nH},$$

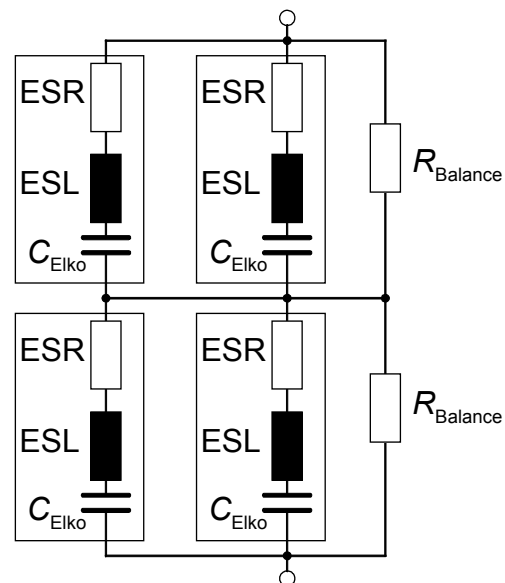
$$L_{CE2} = L_{E1\sigma} + L_{C1\sigma} = L_{sCE} - L_{CE1} = 5.2 \text{ nH}.$$

A passive network is used to model the **tail current**. As shown in Figure 2.9 (a), the current source  $I_{Tail0}$  mirrors the current through  $D_{OUT}$ . When this current drops to 0 during turn-off transient, the energy saved in the inductor  $L_{Tail}$  will be dissipated in the resistor  $R_{Tail}$ . The diode  $D_{Tail}$  is providing the freewheel path for the inductor current. The initial value  $I_{Tail0}$  of this first-order network corresponds to the initial value of the tail current. A time constant  $\tau$  is selected by adjusting the values of  $R_{Tail}$  and  $L_{Tail}$ . The current is then sensed from  $R_{Tail}$  and fed back to the IGBT circuit, using a parallel current source  $I_{Tail}$ . The circuit model for the tail current of the anti-parallel diode is based on the same principle (see the "D\_Tail" indices for corresponding passive network components). The tail-current effect of the anti-parallel diode is noticed especially at high junction temperatures.

Table 2.2: DC-link stray elements

ESR = 190 m $\Omega$
ESL = 20 nH
$C_{Elko} = 470 \mu\text{F}$
$R_{Balance} = 300 \text{ k}\Omega$
$L_{\sigma \text{ DC-link } 1} \approx 29 \text{ nH}$
$L_{\sigma \text{ DC-link } 2} \approx 35.1 \text{ nH}$
$L_{\sigma \text{ DC-link } 3} \approx 34.9 \text{ nH}$
$L_{\sigma \text{ DC-link } 4} \approx 52.3 \text{ nH}$

Figure 2.17: DC-link capacitor HF-model



The selected type of IGBT (FS35R12YT3) has a trench field-stop structure and therefore is designed for a very low tail-current behavior. Thus, it is difficult to estimate the parameters for the tail-current effect. From measurements, a small time constant  $\tau = 30 \text{ ns}$

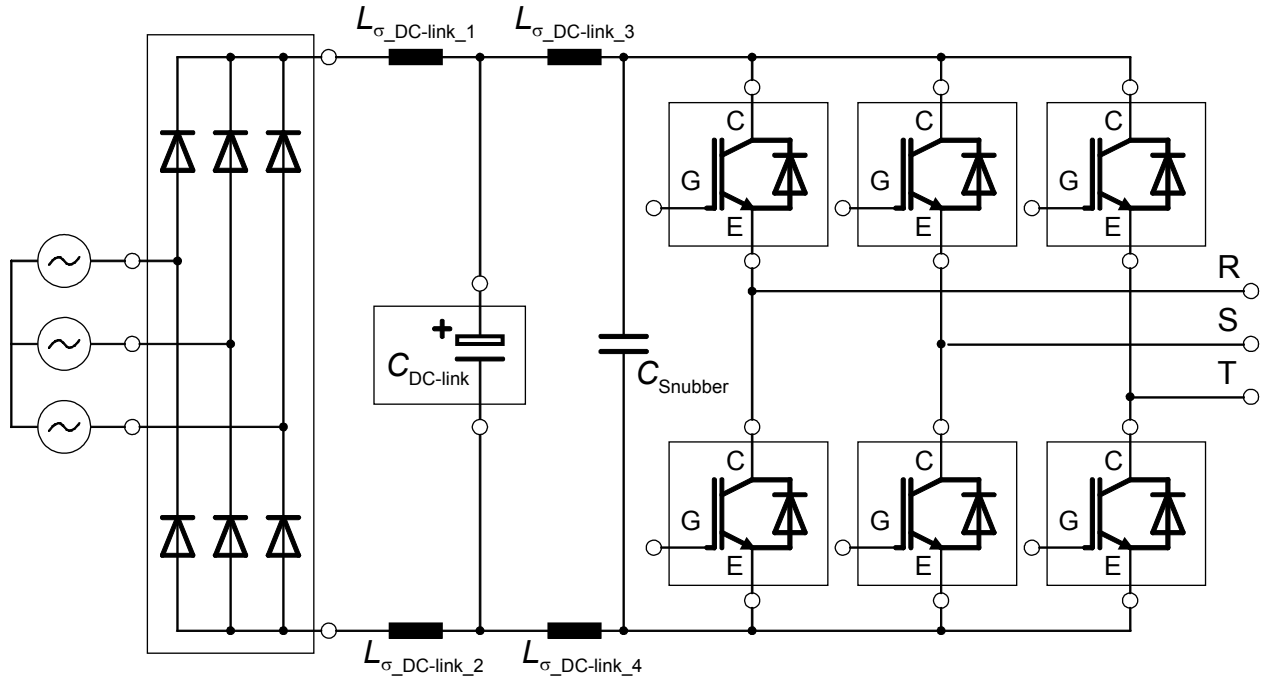


Figure 2.18: Complete inverter model

was determined. For the anti-parallel diode, the tail-current behavior can be neglected, especially in the case of a long cable connection, because the current is oscillating at the inverter output, see Figure 2.21 (b) in section 2.2.1.

### 2.1.3 DC link high-frequency parameters

The stray elements in the DC link have an important influence on the switching waveforms. Figure 2.17 presents the distribution of the parasitic elements for the DC-link capacitors. An arrangement of 4 electrolytic capacitors (2 capacitors in series and 2 branches in parallel) was chosen. The resistors  $R_{\text{Balance}}$  are used to provide an equal voltage sharing between the series-connected capacitors.

Each capacitor can be modeled in HF domain with an additional equivalent-series inductor ESL and an additional equivalent-series resistor ESR. These values can be taken from data sheets [44]. Together with the stray inductance of copper connections, between DC link and IGBT module ( $L_{\sigma\_DC\text{-link}_3}$  and  $L_{\sigma\_DC\text{-link}_4}$  from Figure 2.18), the ESL has a great influence on the voltage waveforms during turn-on and turn-off, when a high  $dI/dt$  occurs.

To avoid this effect, a parallel film-capacitor  $C_{\text{Snubber}}$  is connected as close as possible to the IGBT input terminals. The film capacitors (also called snubber capacitors) have a much smaller ESL than the electrolytic ones. By placing them close to the IGBT terminals, the effect of the stray inductances is reduced. Table 2.2 summarizes the values of the stray elements for the designed DC link. More details about the DC link are offered in subchapter 3.1.

### 2.1.4 Complete inverter HF-model

Finally, the inverter HF-model is built by connecting six IGBT models, the DC-link model and the rectifier bridge. The complete equivalent circuit is presented in Figure 2.18. The individual IGBT equivalent circuits, according to Figure 2.9 (a), are compressed into a sub-model. The electrolytic capacitors, modeled together with the stray elements, are connected via copper stray inductances  $L_{\sigma\_DC\text{-link}_3}$  and  $L_{\sigma\_DC\text{-link}_4}$  to the inverter bridge [45]. Six diodes constitute the rectifier bridge at the inverter input, which is further connected to the DC-link electrolytic capacitors through  $L_{\sigma\_DC\text{-link}_1}$  and  $L_{\sigma\_DC\text{-link}_2}$ .

## 2.2 Cable simulation model

The effect of traveling waves along the cable is well known since the early years of electrical engineering [46]. This phenomenon was studied especially for transmission-line systems for electric energy. Due to the long distances and the high-voltage levels, the study of traveling waves phenomena is becoming important. Voltage surges, e.g. caused by lightning strikes on simple overhead transmission lines, propagate along the line and reflect at the end of the line, leading to the destruction of the connected devices, if no protection devices, like voltage arresters, are used. Also, for small power transmission systems, like data communication, the effect of traveling waves is known. For example, a cable terminator, which equals the cable impedance, is always used in computer networks with coaxial cables (10Base2 or 10Base5) or twisted pair cables (10BaseT or successors). Thus, the wave reflections are damped and an undisturbed communication is assured.

The same principle applies for the inverter-fed motors. Roughly approximated, when the traveling time of the voltage wave exceeds the rise time of the output voltage, the voltage reflections occur at the cable end if the output impedance is larger than the cable impedance. Two major approaches can be found in literature: the transmission line model [29], where the cable is considered as a transfer function and the wave is transmitted between the terminals; the lumped-parameter model which uses a ladder equivalent circuit to simulate the traveling wave [31].

### 2.2.1 Transmission-line model

In [29] and [39], the so-called “bounce diagram”, which represents a particular case of the well-known Bewley diagram [30], is presented. The propagation of the incident and the reflected voltage waves is considered as a function of both time and space. This model is very intuitive to understand the phenomenon of traveling wave. The setup from Figure 2.19 is considered, where a voltage source injects a voltage waveform along the cable (cable impedance  $Z_C$ ). A load with impedance  $Z_L$  is connected at the other end of the cable.

Figure 2.20 shows the bounce diagram. The cable length is  $l$  and the propagation delay of the wave, from one end to the other, is  $t_p = l \cdot \sqrt{L' \cdot C'}$ . The cable is assumed to have no dispersions (losses).  $L'$  and  $C'$  are the phase inductance and capacitance of the cable per unit length, respectively. The inverter impresses a voltage  $V(t)$  to the cable, which is transformed in the Laplace domain  $V(s)$ . Starting from  $t = 0$  and  $x = 0$  (inverter side), the voltage waveform  $V_1$  travels through the cable, Eq. 2.17. At  $t = t_p$ , the first incident wave arrives at the cable end, delayed by the exponential function. Here, a reflection with the coefficient  $K_L$  occurs and the wave travels back to the inverter, Eq. 2.18. The reflection coefficient will depend on the cable and load impedances, Eq. 2.19.

$$V_1(x, s) = V(s) \cdot e^{-\frac{x}{l} t_p \cdot s}, \quad \text{Eq. 2.17}$$

$$V_2(x, s) = K_L \cdot V(s) \cdot e^{-2t_p \cdot s} \cdot e^{\frac{x}{l} t_p \cdot s}, \quad \text{Eq. 2.18}$$

$$K_L = \frac{Z_L - Z_C}{Z_L + Z_C}. \quad \text{Eq. 2.19}$$

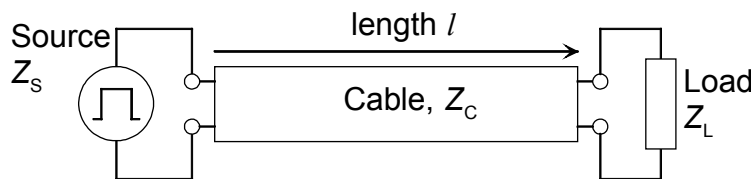
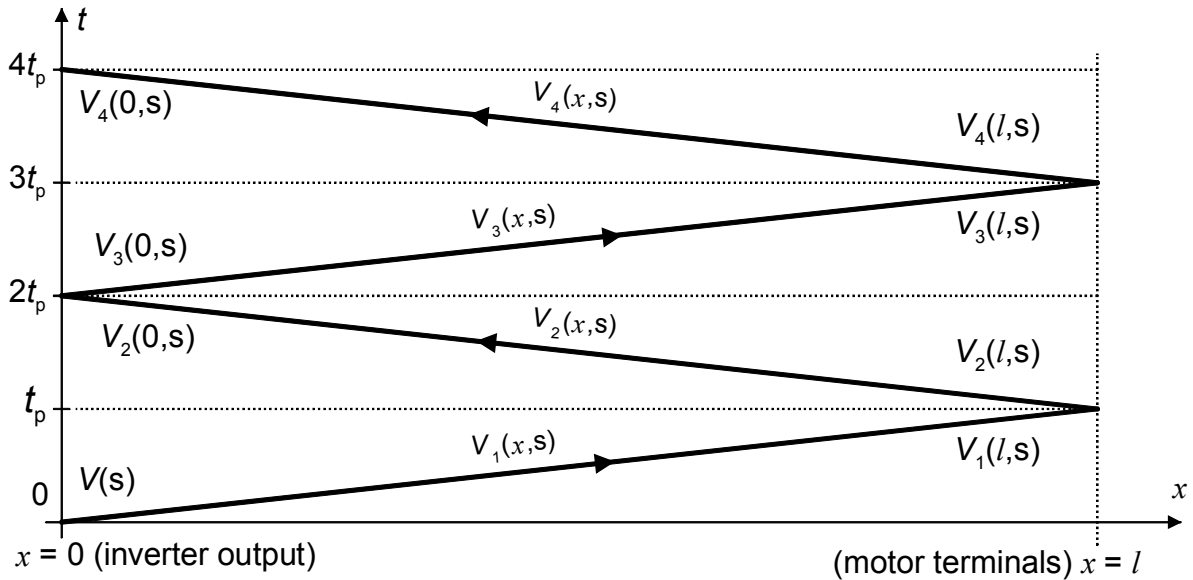


Figure 2.19: Transmission line setup



**Figure 2.20: Transmission line bounce diagram between source and load**

At time  $t = 2t_p$ ,  $V_2$  reaches at the source side and reflects with a different coefficient  $K_S$ , resulting in a new wave  $V_3$ , that travels from source to load:

$$V_3(x, s) = K_S K_L \cdot V(s) \cdot e^{-2t_p \cdot s} \cdot e^{-\frac{x}{l} t_p \cdot s}. \quad \text{Eq. 2.20}$$

The reflection coefficient depends on the source and cable impedances:

$$K_S = \frac{Z_S - Z_C}{Z_S + Z_C}. \quad \text{Eq. 2.21}$$

Propagating for the second time from source to load, the traveling wave reaches the load side of the cable at the time instant  $t = 3t_p$  and will reflect again with the coefficient  $K_L$ . Traveling from load back to the inverter side for the second time, the wave  $V_4$  reaches at inverter at time  $t = 4t_p$ :

$$V_4(x, s) = K_S K_L^2 \cdot V(s) \cdot e^{-4t_p \cdot s} \cdot e^{-\frac{x}{l} t_p \cdot s}. \quad \text{Eq. 2.22}$$

In this way, the voltage on the cable is represented as a sum of infinite reflections. In VSI drives, the inverter represents the voltage source and the motor is connected at the other end of the cable as load. The inverter can be seen as a short circuit, connecting either plus or minus of the DC link to output. Therefore the inverter impedance is very small ( $Z_S \approx 0$ ). On the contrary, the motor input impedance is larger than the cable impedance, especially for low-power motors. This leads to the following condition:  $Z_L \gg Z_C$ . Inserting these conditions in Eq. 2.21 and Eq. 2.19 we obtain:

$$K_S \approx -1 \text{ and } K_L \approx 1.$$

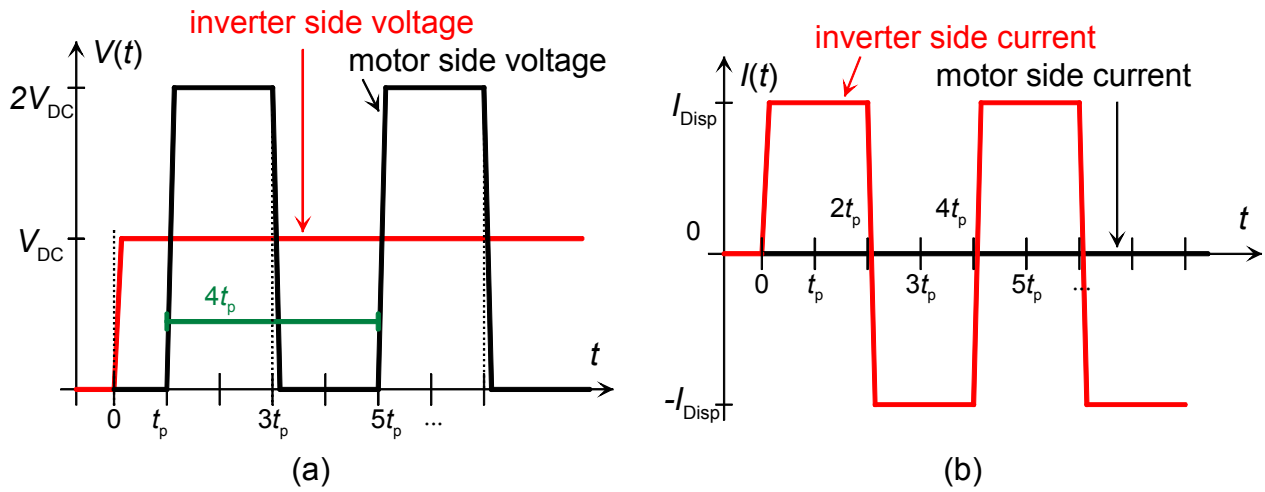
By adding the incident and the reflected voltages at the motor terminals we get:

$$V(l, s) \Big|_{t=t_p} = V_1(l, s) + V_2(l, s) = (1 + K_L) \cdot V(s) \cdot e^{-t_p \cdot s} \approx 2 \cdot V(s) \cdot e^{-t_p \cdot s}.$$

The voltage has double amplitude and is delayed with  $t_p$  time interval. This corresponds to the time instant  $t_p$ , in Figure 2.21 (a). The time reference ( $t = 0$ ) is set at the time instant where the inverter output voltage starts to increase. Further change in the motor voltage occurs at time instant  $3t_p$ , where the voltage has the expression:

$$V(l, s) \Big|_{t=3t_p} = V(l, s) \Big|_{t=t_p} + V_3(l, s) + V_4(l, s) = V(l, s) \Big|_{t=t_p} + (K_S K_L + K_S K_L^2) \cdot V(s) \cdot e^{-3t_p \cdot s} \approx 0$$

and will reach the  $2V_{DC}$  value again at time instant  $5t_p$ . Thus, the voltage will oscillate at the motor terminals with the period  $4t_p$ , see Figure 2.21 (a). In a similar way, the voltage at the inverter output can be calculated. The voltage waveform  $V(s)$  is injected to the cable at



**Figure 2.21: Theoretical waveforms for voltage (a) and HF-current (b) at ideal cables**

time  $t = 0$ . After reflecting at the motor side, the wave reaches the inverter and reflects with the coefficient  $K_S$ , generating the total voltage at the inverter terminals:

$$V(0,s)|_{t=2t_p} = V(s)|_{t=0} + V_2(0,s) + V_3(0,s) = (1 + K_L + K_S K_L) \cdot V(s) \cdot e^{-2t_p \cdot s} \approx V(s) \cdot e^{-2t_p \cdot s}.$$

It can be noticed that the voltage amplitude remains the same also at  $t = 2t_p$ . Further, after traveling four times from inverter to motor and back, the voltage waveform is:

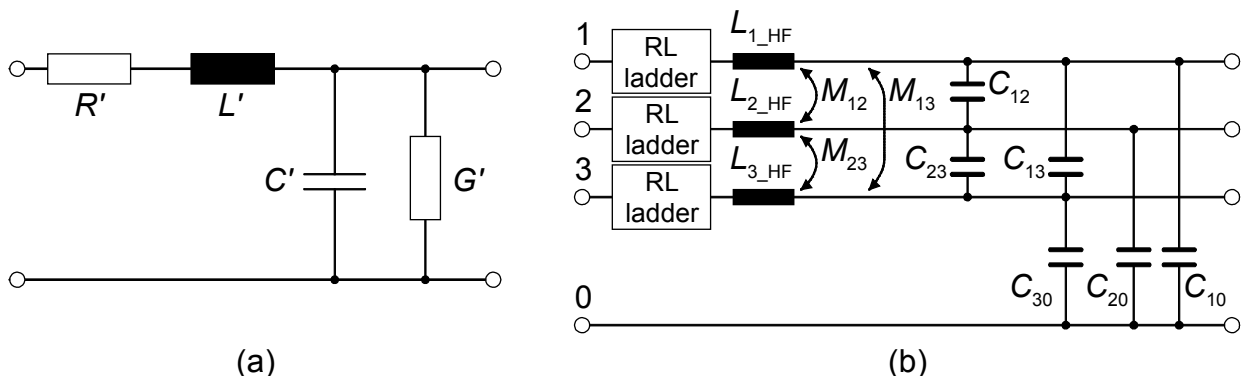
$$V(0,s)|_{t=4t_p} = V(s)|_{t=2t_p} + V_4(0,s) + V_5(0,s) = (1 + K_S K_L^2 + K_S^2 K_L^2) \cdot V(s) \cdot e^{-4t_p \cdot s} \approx V(s) \cdot e^{-4t_p \cdot s}.$$

In conclusion it can be said, that the reflection coefficient  $K_L \approx 1$  determines at the motor terminals voltage oscillations with double amplitude. The reflection coefficient  $K_S \approx -1$  leads at the inverter side to no voltage oscillations, see Figure 2.21 (a).

The successive voltage gradients will determine displacement currents in the cable stray capacitances. Thus, current traveling waves are also impressed to the cable, oscillating at inverter side with twice the displacement current amplitude  $I_{Disp}$  and no oscillating at the motor side, due to current reflection coefficients  $K_S$  and  $K_L$ , see Figure 2.21 (b). Assuming the same relations between the inverter, cable and motor impedances in VSIs ( $Z_S \approx 0$  and  $Z_L \gg Z_C$ ), these coefficients are finally approximated as shown earlier:  $K_S \approx -1$  and  $K_L \approx 1$ .

## 2.2.2 Lumped-parameter model

Despite the fact that the transmission-line model, presented above, is easy to implement and allows fast simulations, it cannot describe entirely the internal phenomena of the cable such as: mutual coupling between individual cable conductors, capacitive couplings between two conductors and between each conductor and earth, cable



**Figure 2.22:  $\Gamma$  equivalent circuit for lumped parameter cable model (a) and 3-phase cable model (b)**

asymmetries due to different layouts, cable losses at high frequencies due to skin and proximity effects, etc. Therefore, a more complex model is required. This can be achieved with a lumped-parameter model, where the cable is regarded as a ladder connection of individual  $\Gamma$  equivalent circuits. Such an equivalent circuit is shown in Figure 2.22 (a).  $R'$  and  $L'$  represent the phase resistance and inductance of copper string per unit length.  $C'$  and  $G'$  stand for capacitance and conductance per unit length between line and ground.

Connecting three  $\Gamma$  circuits, like in Figure 2.22 (b), an equivalent circuit for the three-phase transmission system (cable) is obtained. Here, the conductance between two wires is neglected because is very small ( $G_{ij} \approx 0$ ). Moreover, additional components are considered: the inductive coupling between conductors represented by  $M_{ij}$ ; the capacitive coupling between conductors simulated with  $C_{ij}$ ; the capacitive coupling between each conductor and ground represented by  $C_{i0}$ , ( $i$  and  $j = 1 \dots 3$  stand for conductor number). The inductances for Protective Earth (PE) and shield are neglected, because they carry a current much smaller (ideally zero) than the load current.

Additionally, RL ladder blocks are used to simulate the skin and proximity effects at high frequencies. These will determine a resistance and inductance variation with frequency. More details will be given in section 2.2.5. The remaining inductance  $L_{LHF}$  represents the longitudinal inductance of the conductor, measured at high frequency.

The model is developed as a connection of several equivalent  $\Gamma$  circuits in a ladder structure. The number of chosen  $\Gamma$  circuits determines the quality of the simulated waveforms, i.e. a bigger number leads to a better accuracy. The parameters of a single  $\Gamma$  circuit have normalized values, depending on the chosen length of the  $\Gamma$  section.

To determine the minimum necessary number of  $\Gamma$  sections for a desired accuracy, following consideration is made: the voltage waveform is simplified using a trapezoidal function; see Figure 2.24 (a). The characteristics of the waveform are: the rise time  $t_r$  and the period  $T$ . The period is assumed to be much larger than the rise time ( $T \gg t_r$ ), usually being around the inverse of a few kHz (IGBT switching frequency). Thus, a Fourier analysis shows that the voltage harmonics, which have to be considered, exists mainly in the frequency range  $f_s < f < f_{co}$ , where  $f_{co}$  stands for cutoff frequency. Assuming a low-loss cable ( $R' \ll X_L'$ ), the cutoff frequency equals the resonance frequency of the cable [47]:

$$f_{co} = \frac{\omega_{co}}{2\pi} \approx f_0 = \frac{\omega_0}{2\pi} = \frac{\pi / (2 \cdot l \cdot \sqrt{L' C'})}{2\pi} = \frac{1}{4 \cdot l \cdot \sqrt{L' C'}}. \quad \text{Eq. 2.23}$$

If  $R'$ ,  $L'$  and  $C'$  are assumed to be frequency independent, then the cable transmission is linear, allowing all harmonic components to travel with the same speed  $v_C$ . The propagation speed of the wave is given by:

$$v_C = \frac{1}{\sqrt{L' \cdot C'}} = \frac{l}{t_p}, \text{ where } l \text{ represents the total length of the cable.} \quad \text{Eq. 2.24}$$

For simplifications, the cutoff frequency is roughly approximated in direct relation to the highest harmonic given by the rise time:  $f_{co} \approx 1/t_r$  [34]. Further, the wavelength associated to a waveform depends on the cable parameters (for low-loss cables) [47]:

$$\lambda = \frac{2\pi}{\beta} = \frac{2\pi}{\omega \sqrt{L' C'}}, \quad \text{Eq. 2.25}$$

where  $\beta$  is the phase constant of the voltage wave. The smallest wavelength of the highest harmonic is obtained by including Eq. 2.23 and Eq. 2.24 in Eq. 2.25:

$$\lambda_{min} = \frac{2\pi}{\omega_{co} \sqrt{L' C'}} = \frac{v_C}{f_{co}} = v_C \cdot t_r. \quad \text{Eq. 2.26}$$

In [48], the critical length is determined as a function of minimal wavelength of the fastest transient and desired accuracy, namely the relation between the variation of the electrical field  $dE$ , along the length of the  $\Gamma$  segment, and electric field at segment input  $E$ :

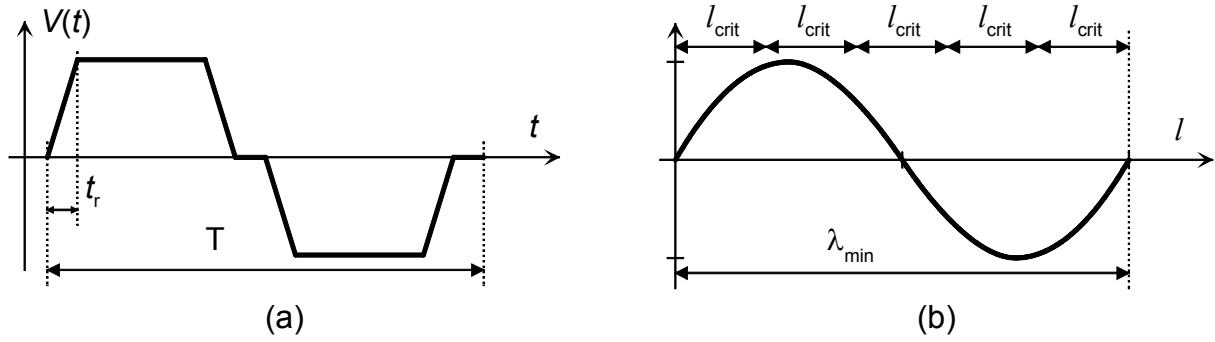


Figure 2.24: Assumed voltage signal (a) and sinus wave of highest relevant harmonic

$$l_{\text{crit}} = \left( \frac{dE}{E} \right)_{\text{desired}} \cdot \frac{\lambda_{\min}}{2\pi} = \frac{\lambda_{\min}}{5} \dots \frac{\lambda_{\min}}{10}. \quad \text{Eq. 2.27}$$

Inserting Eq. 2.26 in Eq. 2.27, the relation for the critical length is obtained:

$$l_{\text{crit}} = \left( \frac{dE}{E} \right)_{\text{desired}} \cdot \frac{V_C \cdot t_r}{2\pi}. \quad \text{Eq. 2.28}$$

By analyzing the sinus wave of the highest harmonic, one can say that a sinus can be approximated using at least 4 points, see Figure 2.24 (b). Therefore, a minimum number of 5 segments should be chosen. However, in [49] a factor of 10 segments per minimum wavelength is suggested. Concluding, it can be said that the selection of the number of segments is a compromise between the desired accuracy and the simulation burden. An increased number of segments leads automatically to longer simulation times. But there is also a limit, namely the minimum segment length should always be always five times less than the minimum wavelength  $\lambda_{\min}$ . The minimum wavelength corresponds to the highest-order harmonic of the voltage waveform.

Another important aspect, regarding the relation between cable length, transient time and voltage amplitude at the motor terminals, was given in literature. The equations in Laplace domain for the reflected voltage at motor terminals were presented previously in Eq. 2.17 - Eq. 2.22. An essential condition for voltage amplitude of 2 pu is found in [31]:

$$V_{\text{mot\_peak}} = V_{\text{mot}} \Big|_{t=t_p} = V_{\text{DC}} \cdot (1 + (t_p / t_r) \cdot K_L), \text{ for } t_p < t_r \text{ and} \quad \text{Eq. 2.29}$$

$$V_{\text{mot\_peak}} = V_{\text{mot}} \Big|_{t=t_p} = V_{\text{DC}} \cdot (1 + K_L), \text{ for } t_p \geq t_r. \quad \text{Eq. 2.30}$$

### 2.2.3 Parameter identification – Capacitances

The cable partial capacitances can be determined using analytical calculations, finite

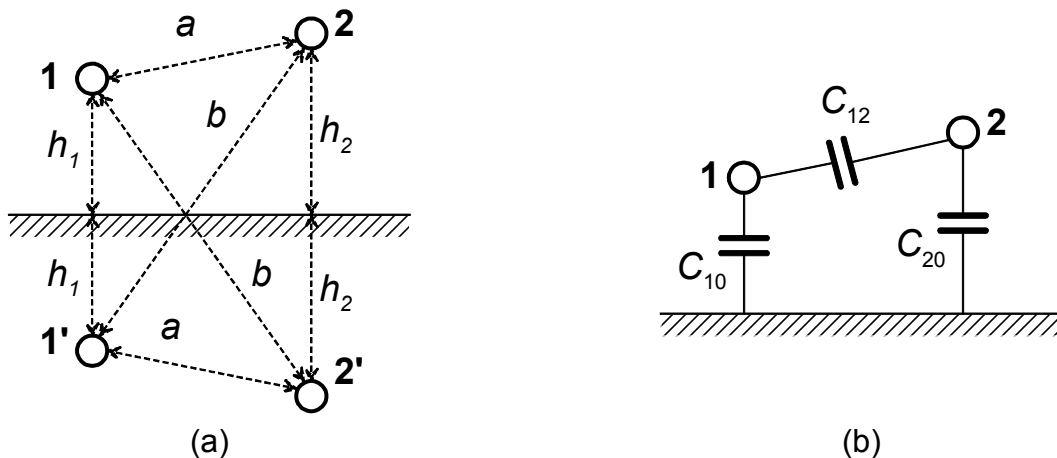


Figure 2.23: Conductors in free air: mirror image configuration (a) and partial capacitances (b)



element simulations or direct measurements on a piece of cable. The first and the latter will be detailed further. Different cable configurations are investigated to show the reliability of the chosen methods. Also, for different cable layouts (ground displacement) and asymmetries (different distances between conductors), several approaches are used for the cable analysis.

The **analytical calculation** of the cable partial capacitances is based on the mirror-image method [50]. The main idea consists in superposition of the individual potentials when the electric field is not disturbed. For exemplification, the simple case of two conductors (1 and 2) is analyzed (Figure 2.23). Considering the cross section of the conductors, they can be replaced by the circular charge sources  $Q_1$  and  $Q_2$ . A homogenous equipotential surface represents the ground plane. The mirror images of each electric source are located with respect to the equipotential surface (1' and 2') and have reversed polarity as the original sources (i.e.  $-Q_1$  and  $-Q_2$ ). The distances between the two electro-static sources and ground plane are shown in Figure 2.23 (a). The configuration of the partial capacitances is presented in Figure 2.23 (b): between the conductors ( $C_{12}$ ) and between conductors and ground ( $C_{10}$  and  $C_{20}$ ).

Based on the geometrical configuration from Figure 2.23 (a), following potential equations are considered, regarding the conductor diameters  $d_1$  and  $d_2$ , respectively:

$$\begin{aligned}\varphi_1 &= \frac{1}{2\pi\epsilon_0 l} \left[ Q_1 \ln \frac{4h_1}{d_1} + Q_2 \ln \frac{b}{a} \right] \\ \varphi_2 &= \frac{1}{2\pi\epsilon_0 l} \left[ Q_1 \ln \frac{b}{a} + Q_2 \ln \frac{4h_2}{d_2} \right]\end{aligned}\quad \text{Eq. 2.31}$$

where a homogenous air space between conductors is assumed, and  $l$  is the considered length of the section. Usually  $l$  is considered 1 meter for simplifications of the calculations. Solving the equation system Eq. 2.31 for  $Q_1$  and  $Q_2$ , we obtain:

$$\begin{aligned}Q_1 \left[ \ln \frac{4h_1}{d_1} \ln \frac{4h_2}{d_2} - \ln^2 \frac{b}{a} \right] &= 2\pi\epsilon_0 l \left[ \varphi_1 \ln \frac{4h_2}{d_2} - \varphi_2 \ln \frac{b}{a} \right] \\ Q_2 \left[ \ln \frac{4h_1}{d_1} \ln \frac{4h_2}{d_2} - \ln^2 \frac{b}{a} \right] &= 2\pi\epsilon_0 l \left[ \varphi_2 \ln \frac{4h_1}{d_1} - \varphi_1 \ln \frac{b}{a} \right]\end{aligned}\quad \text{Eq. 2.32}$$

The electric charge for conductor 1 is a sum of potential differences with respect to the other sources multiplied by the partial capacitances  $C_{12}$ ,  $C_{13}$ ,  $C_{14}$ , etc.:

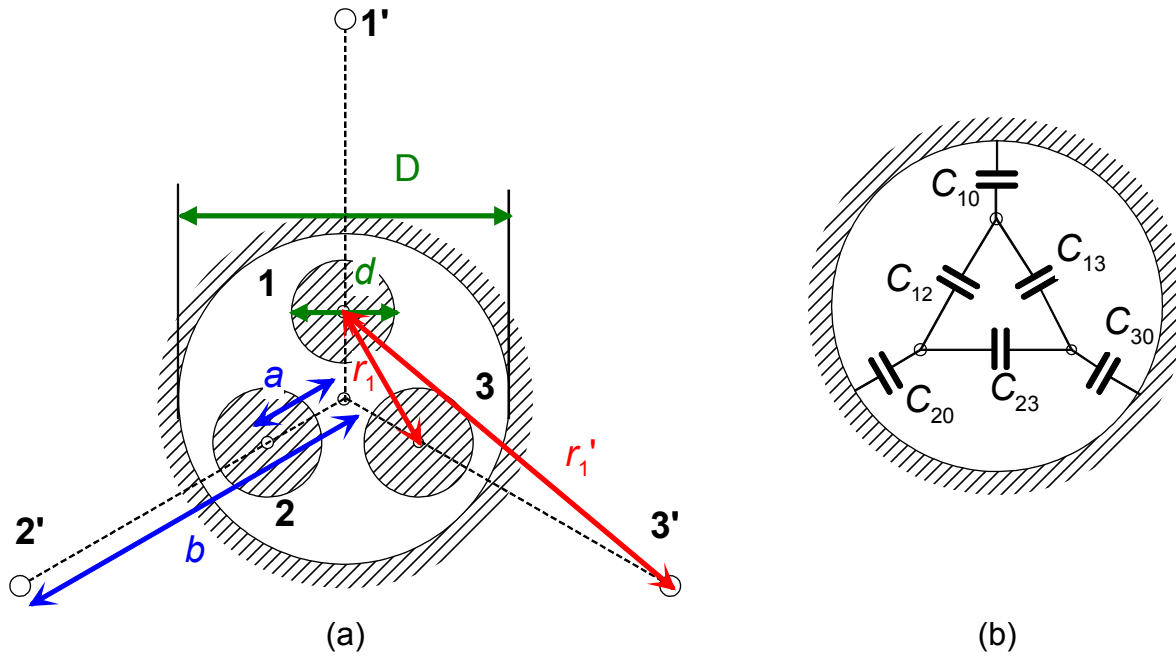
$$Q_1 = C_{12}(\varphi_1 - \varphi_2) + C_{13}(\varphi_1 - \varphi_3) + C_{14}(\varphi_1 - \varphi_4) + \dots \quad \text{Eq. 2.33}$$

Transforming Eq. 2.32 in a similar expression like Eq. 2.33, we obtain:

$$\begin{aligned}Q_1 \left[ \ln \frac{4h_1}{d_1} \ln \frac{4h_2}{d_2} - \ln^2 \frac{b}{a} \right] &= 2\pi\epsilon_0 l \left[ \varphi_1 \left( \ln \frac{4h_2}{d_2} - \ln \frac{b}{a} \right) + (\varphi_1 - \varphi_2) \ln \frac{b}{a} \right] \\ Q_2 \left[ \ln \frac{4h_1}{d_1} \ln \frac{4h_2}{d_2} - \ln^2 \frac{b}{a} \right] &= 2\pi\epsilon_0 l \left[ \varphi_2 \left( \ln \frac{4h_1}{d_1} - \ln \frac{b}{a} \right) + (\varphi_2 - \varphi_1) \ln \frac{b}{a} \right]\end{aligned}\quad \text{Eq. 2.34}$$

from which, the expressions of the partial capacitances can be extracted:

$$\begin{aligned}C_{10} &= 2\pi\epsilon_0 l \frac{\ln(4h_2/d_2) - \ln(b/a)}{\ln \frac{4h_1}{d_1} \ln \frac{4h_2}{d_2} - \ln^2 \frac{b}{a}}, \quad C_{20} = 2\pi\epsilon_0 l \frac{\ln(4h_1/d_1) - \ln(b/a)}{\ln \frac{4h_1}{d_1} \ln \frac{4h_2}{d_2} - \ln^2 \frac{b}{a}} \text{ and} \\ C_{12} &= 2\pi\epsilon_0 l \frac{\ln(b/a)}{\ln \frac{4h_1}{d_1} \ln \frac{4h_2}{d_2} - \ln^2 \frac{b}{a}}.\end{aligned}$$



**Figure 2.25: Three-phase cable: mirror images configuration (a) and partial capacitances (b)**

The phase capacitance is defined as the equivalent capacitance of the entire system depending on the application type [50]. For example, in Figure 2.23 (b) two applications are analyzed: **case1** when the voltage waveform is applied between the two conductors and **case2** when voltage waveform is injected between conductor 1 and ground.

$$C_{\text{ph\_case1}} = C_{12} + \frac{C_{10}C_{20}}{C_{10} + C_{20}} \quad \text{and} \quad C_{\text{ph\_case2}} = C_{10} + \frac{C_{12}C_{20}}{C_{12} + C_{20}}.$$

Particular cases may be derived when certain conditions are imposed:

- 2 conductors in air far from equipotential surface ( $h_x \gg d_x$ ) leads to negligible conductor-earth capacitances;
- the same distance between conductors and ground ( $h_x = d_x$ ) determines simplified relations for the partial and the phase capacitances.

Another theoretical example is offered in [50] regarding a shielded three-phase cable (3 conductors). Here, the equipotential surface is no longer a plane but surrounds the conductors. The geometrical configuration for the mirror-image method is shown in Figure 2.25 (a). The conductors are similar in this case (same diameter  $d$ ), the distance between the center of the conductor and the center of the cable is  $a$ , while the shield has the diameter  $D$ . The mirror images are located at the distance  $b = D^2 / 4a$  and the medium between conductors is no longer air. Thus, the distances  $r_1$  and  $r_1'$  must be determined for the calculation of the partial capacitances from Figure 2.25 (b):

$$r_1 = a\sqrt{3}; \quad r_1' = \sqrt{a^2 + b^2 + ab}. \quad \text{Eq. 2.35}$$

Using Eq. 2.35, the system of equations for the electro-static potentials is obtained:

$$\begin{aligned} \varphi_1 &= \frac{1}{2\pi\epsilon \cdot l} \left[ Q_1 \ln 2 \frac{b-a}{d} + Q_2 \ln \frac{\sqrt{a^2 + b^2 + ab}}{a\sqrt{3}} + Q_3 \ln \frac{\sqrt{a^2 + b^2 + ab}}{a\sqrt{3}} \right] \\ \varphi_2 &= \frac{1}{2\pi\epsilon \cdot l} \left[ Q_1 \ln \frac{\sqrt{a^2 + b^2 + ab}}{a\sqrt{3}} + Q_2 \ln 2 \frac{b-a}{d} + Q_3 \ln \frac{\sqrt{a^2 + b^2 + ab}}{a\sqrt{3}} \right] \\ \varphi_3 &= \frac{1}{2\pi\epsilon \cdot l} \left[ Q_1 \ln \frac{\sqrt{a^2 + b^2 + ab}}{a\sqrt{3}} + Q_2 \ln \frac{\sqrt{a^2 + b^2 + ab}}{a\sqrt{3}} + Q_3 \ln 2 \frac{b-a}{d} \right] \end{aligned} \quad \text{Eq. 2.36}$$

The potential of the shield can be defined as:

$$\varphi_0 = \frac{1}{2\pi\epsilon \cdot l} (Q_1 + Q_2 + Q_3) \ln \frac{D}{2a}. \quad \text{Eq. 2.37}$$

Under the consideration of the potential difference, a variable change is used:  $V_i = \varphi_i - \varphi_0$ . Inserting Eq. 2.37 in Eq. 2.36 the system of equations for potential differences can be written:

$$\begin{aligned} V_1 = \varphi_1 - \varphi_0 &= \frac{1}{2\pi\epsilon \cdot l} \left[ Q_1 \ln \frac{4a(b-a)}{Dd} + (Q_2 + Q_3) \ln \frac{2\sqrt{a^2 + b^2 + ab}}{D\sqrt{3}} \right] \\ V_2 = \varphi_2 - \varphi_0 &= \frac{1}{2\pi\epsilon \cdot l} \left[ Q_2 \ln \frac{4a(b-a)}{Dd} + (Q_1 + Q_3) \ln \frac{2\sqrt{a^2 + b^2 + ab}}{D\sqrt{3}} \right], \\ V_3 = \varphi_3 - \varphi_0 &= \frac{1}{2\pi\epsilon \cdot l} \left[ Q_3 \ln \frac{4a(b-a)}{Dd} + (Q_1 + Q_2) \ln \frac{2\sqrt{a^2 + b^2 + ab}}{D\sqrt{3}} \right] \end{aligned} \quad \text{Eq. 2.38}$$

and in matrix form:

$$\mathbf{V} = \mathbf{K} \cdot \mathbf{Q},$$

where  $\mathbf{K}$  represents the coefficient matrix and depends on the geometrical construction. The following simplification will be considered due to the cable layout: the capacitances between conductors and shield are set equal  $C_0 = C_{10} = C_{20} = C_{30}$  and between two conductors also  $C_1 = C_{12} = C_{23} = C_{13}$ .

By extending Eq. 2.33, the electric charge is obtained as a function of partial capacitances and potential differences:

$$Q_1 = V_1 C_0 + (V_1 - V_2) C_1 + (V_1 - V_3) C_1$$

$$Q_2 = V_2 C_0 + (V_2 - V_1) C_1 + (V_2 - V_3) C_1,$$

$$Q_3 = V_3 C_0 + (V_3 - V_1) C_1 + (V_3 - V_2) C_1$$

Eq. 2.39

and in matrix form:

$$\mathbf{Q} = \mathbf{C} \cdot \mathbf{V}.$$

Multiplying Eq. 2.39 with the inverse of the capacitance matrix  $\mathbf{C}^{-1}$ , we get:

$$\mathbf{V} = \mathbf{C}^{-1} \cdot \mathbf{Q},$$

Eq. 2.40

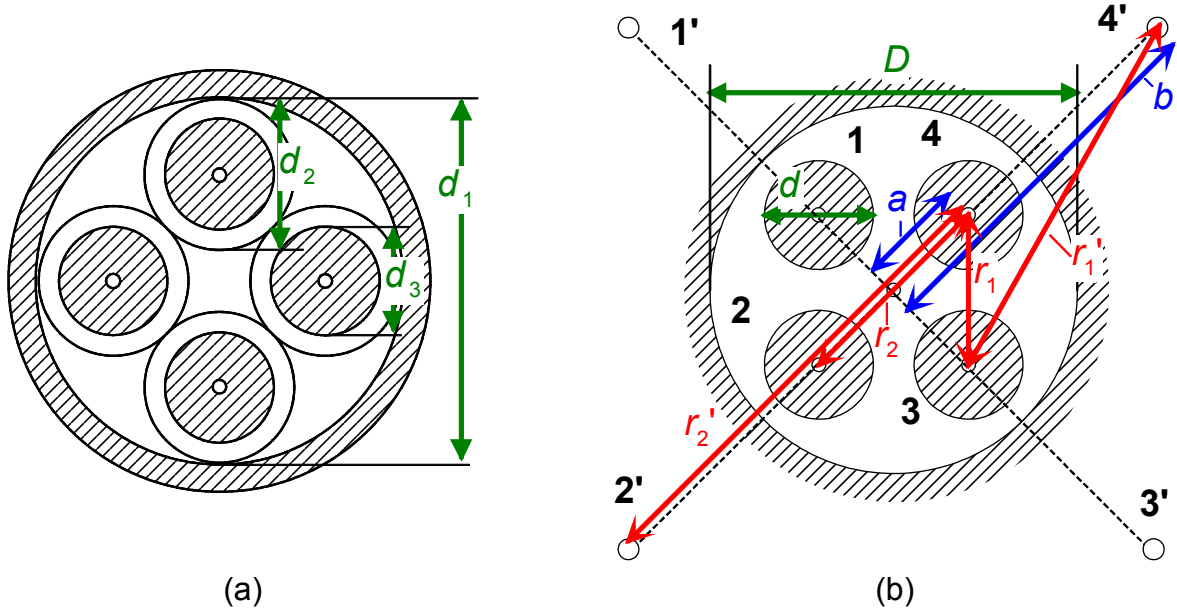
and comparing Eq. 2.40 with Eq. 2.38, the partial capacitances are obtained from the coefficient matrix  $\mathbf{K}$ :

$$C_0 = 2\pi\epsilon \cdot l \frac{1}{\ln \frac{16a(b^3 - a^3)}{3D^3d}}; \quad C_1 = 2\pi\epsilon \cdot l \frac{\ln \frac{4a(a^2 + b^2 + ab)}{3D^2}}{\ln \frac{12a^2(b-a)^2}{d^2(a^2 + b^2 + ab)} \cdot \ln 2 \frac{16a(b^3 - a^3)}{3D^3d}}.$$

### 2.2.3.1 Shielded cables with more than 3 conductors

In practice, three-phase cables with only three conductors are used on a small scale. Instead, cables with four and five conductors are met, where additional conductors are used to connect the neutral (N) point and/or the protective earth (PE). To calculate the partial capacitances for this type of cables, the method presented previously has to be adapted to new cable layouts.

First, the case of a **four-conductor cable** is considered. The cable cross-section is shown in Figure 2.26 (a). The three diameters are measured on a cable example (*Motorflex YSLYCY-JZ 600/100V*, 6 mm<sup>2</sup>):  $d_1 = 14.6$  mm,  $d_2 = 5.2$  mm,  $d_3 = 2.8$  mm.



**Figure 2.26: Cross-section of a 4-conductor shielded cable (a) and geometrical configuration (b)**

Based on the physical dimensions, the distances in the geometrical configuration are determined for the mirror-image method, see Figure 2.26 (b). Here, the conductor images are built with respect to shield at the distance  $b = D^2 / 4a$  from the cable center:

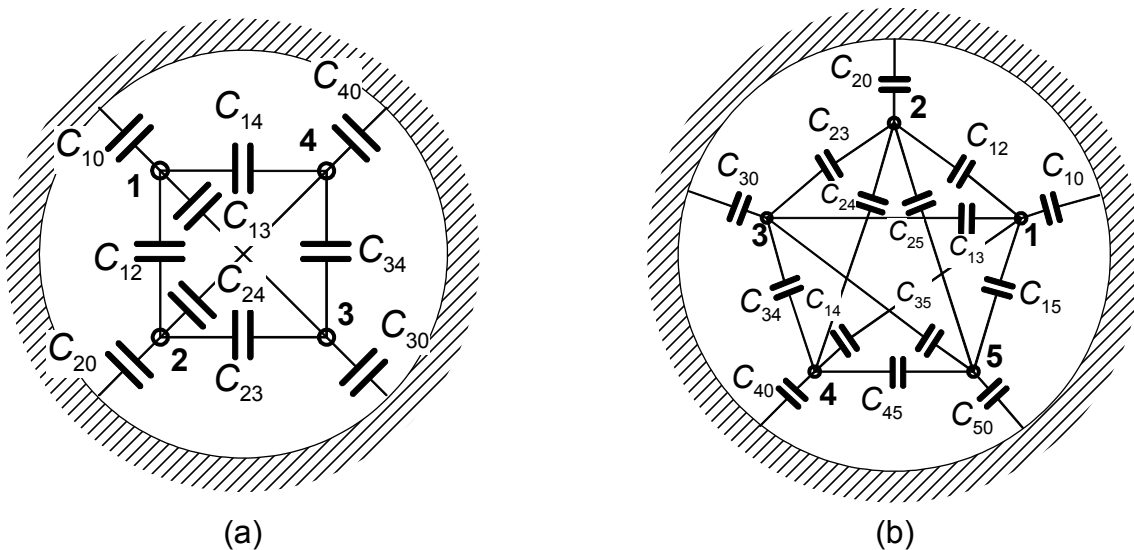
$$r_1 = a\sqrt{2}, \quad r_1' = \sqrt{a^2 + b^2},$$

$$r_2 = 2a, \quad r_2' = a + b.$$

In a similar way like the case with 3-conductor cable, the coefficient matrix is obtained, considering both conductor potential and shield potential. The relation between the potential differences and the electrical charge of conductors can be written in matrix form:

$$\mathbf{V} = \mathbf{K} \cdot \mathbf{Q},$$

where the coefficient matrix  $\mathbf{K}$  has the dimension equal to the number of conductors. The following expression results:



**Figure 2.27: Partial capacitances for 4-conductor (a) and 5-conductor (b) shielded cable**

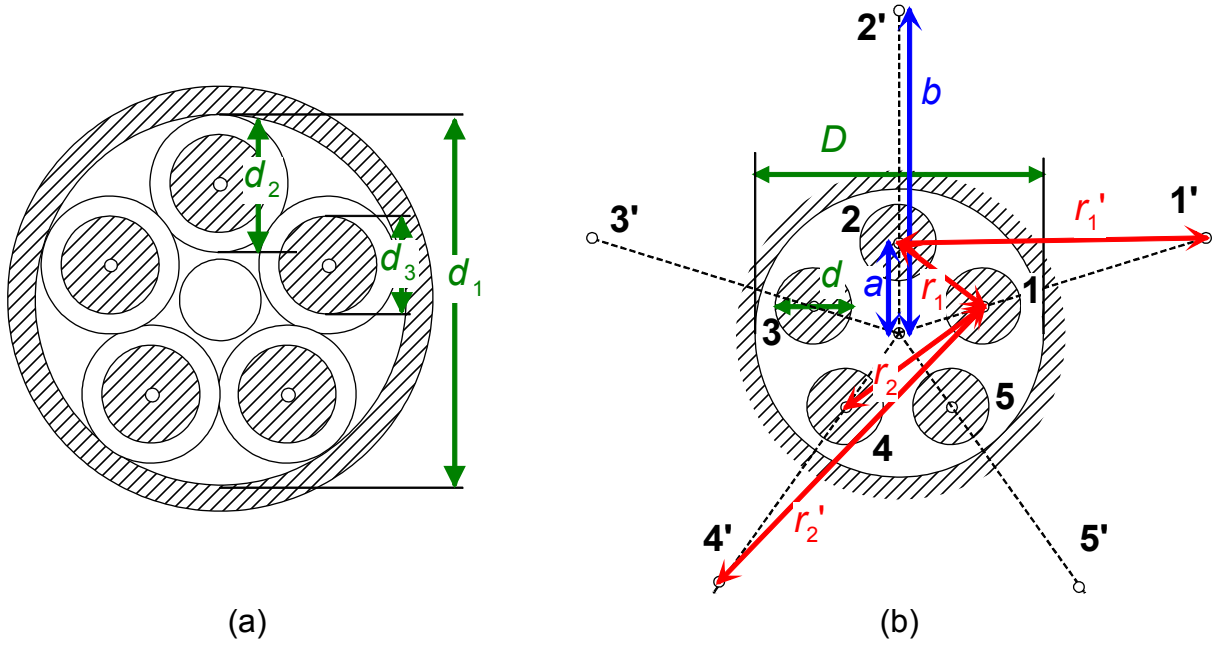


Figure 2.28: 5-conductor shielded cable cross section (a) and geometrical configuration (b)

$$\mathbf{K} = \frac{1}{2\pi\epsilon \cdot l} \begin{bmatrix} \ln \frac{4a(b-a)}{Dd} & \ln \frac{\sqrt{2(a^2+b^2)}}{D} & \ln \frac{a+b}{D} & \ln \frac{\sqrt{2(a^2+b^2)}}{D} \\ \ln \frac{\sqrt{2(a^2+b^2)}}{D} & \ln \frac{4a(b-a)}{Dd} & \ln \frac{\sqrt{2(a^2+b^2)}}{D} & \ln \frac{a+b}{D} \\ \ln \frac{a+b}{D} & \ln \frac{\sqrt{2(a^2+b^2)}}{D} & \ln \frac{4a(b-a)}{Dd} & \ln \frac{\sqrt{2(a^2+b^2)}}{D} \\ \ln \frac{\sqrt{2(a^2+b^2)}}{D} & \ln \frac{a+b}{D} & \ln \frac{\sqrt{2(a^2+b^2)}}{D} & \ln \frac{4a(b-a)}{Dd} \end{bmatrix}.$$

In this case there are three types of partial capacitances: between conductors and shield  $C_0 = C_{10} = C_{20} = C_{30} = C_{40}$ , between two neighbor conductors  $C_1 = C_{12} = C_{23} = C_{34} = C_{14}$  and between two distant conductors  $C_2 = C_{13} = C_{24}$ , see Figure 2.27 (a). The matrix of the partial capacitances has the following expression:

$$\mathbf{C} = \begin{bmatrix} C_0 + 2C_1 + C_2 & -C_1 & -C_2 & -C_1 \\ -C_1 & C_0 + 2C_1 + C_2 & -C_1 & -C_2 \\ -C_2 & -C_1 & C_0 + 2C_1 + C_2 & -C_1 \\ -C_1 & -C_2 & -C_1 & C_0 + 2C_1 + C_2 \end{bmatrix}.$$

Finally, by comparing matrix  $\mathbf{K}$  with matrix  $\mathbf{C}^{-1}$ , the partial capacitances are determined:

$$C_0 = \frac{2\pi\epsilon \cdot l}{\ln \frac{8a(b^2+a^2)(b^2-a^2)}{D^4d}}; C_1 = \frac{\pi\epsilon \cdot l \cdot \ln \frac{2(a^2+b^2)}{D^2}}{\ln \frac{(b^2-a^2)}{(b^2+a^2)} \frac{2a}{d} \cdot \ln \frac{8a(b^2+a^2)(b^2-a^2)}{D^4d}} \text{ and}$$

$$C_2 = \frac{\pi\epsilon \cdot l \cdot \left[ -\ln^2 \frac{2}{D^2} - 4\ln(a^2+b^2)\ln \frac{1}{D} - \ln(a^2+b^2)\ln 4 - \ln^2(a^2+b^2) + 2\ln^2 \frac{a+b}{D} + 2\ln \frac{a+b}{D} \ln \frac{4a(b-a)}{Dd} \right]}{\ln \frac{4a(b-a)}{d(a+b)} \cdot \ln \frac{(b^2-a^2)}{(b^2+a^2)} \frac{2a}{d} \cdot \ln \frac{8a(b^2+a^2)(b^2-a^2)}{D^4d}}.$$

Another case is the use of a **five-conductor cable** (*LAPP Classic 115CY*, 2.5 mm<sup>2</sup>), whose cross section is shown in Figure 2.28 (a):  $d_1 = 8.1$  mm,  $d_2 = 3$  mm,  $d_3 = 1.6$  mm. The distances used for the mirror-image method have the following expression, see Figure 2.28 (b):

$$r_1 = a \cdot 1.18, \quad r_1' = \sqrt{a^2 + b^2 - 0.6 \cdot ab},$$

$$r_2 = a \cdot 1.9, \quad r_2' = 0.9 \cdot a + b.$$

The shield potential in this case is:

$$\varphi_0 = (1/2\pi\epsilon \cdot l)(Q_1 + Q_2 + Q_3 + Q_4 + Q_5)\ln(D/2a),$$

which, inserted in the potentials equation system, similar to Eq. 2.36, determines further the matrix form of the equation system for potential differences  $\mathbf{V} = \mathbf{K} \cdot \mathbf{Q}$ . The coefficient matrix is now expressed as:

$$\mathbf{K} = \frac{1}{2\pi\epsilon \cdot l} \begin{bmatrix} x & y & z & z & y \\ y & x & y & z & z \\ z & y & x & y & z \\ z & z & y & x & y \\ y & z & z & y & x \end{bmatrix},$$

where the matrix elements are:

$$x = \ln \frac{4a(b-a)}{Dd}; \quad y = \ln \frac{2\sqrt{a^2 + b^2 - 0.6ab}}{1.18 \cdot D} \quad \text{and} \quad z = \ln \frac{2(0.9 \cdot a + b)}{1.9 \cdot D}.$$

In this case can be noticed, that the terms of the matrix  $\mathbf{K}$  are slightly different from those in the 4-conductor case. The diagonal term is similar while the off-diagonal terms are slightly differing due to the pentagon cable layout. Also in this case, the matrix dimension is equal to the number of conductors. Now, the partial capacitances (Figure 2.27 (b)) are approximated and their number reduced to three:

- between conductors and shield  $C_0 = C_{10} = C_{20} = C_{30} = C_{40} = C_{50}$ ;
- between two neighbor conductors:  $C_1 = C_{12} = C_{23} = C_{34} = C_{45} = C_{15}$ ;
- between two distant conductors:  $C_2 = C_{13} = C_{14} = C_{24} = C_{25} = C_{35}$ .

Thus, the equation system for electric charge is simplified to:

$$\mathbf{Q} = \mathbf{C} \cdot \mathbf{V},$$

where the matrix of the partial capacitances has the following form:

$$\mathbf{C} = \begin{bmatrix} C_0 + 2C_1 + 2C_2 & -C_1 & -C_2 & -C_2 & -C_1 \\ -C_1 & C_0 + 2C_1 + 2C_2 & -C_1 & -C_2 & -C_2 \\ -C_2 & -C_1 & C_0 + 2C_1 + 2C_2 & -C_1 & -C_2 \\ -C_2 & -C_2 & -C_1 & C_0 + 2C_1 + 2C_2 & -C_1 \\ -C_1 & -C_2 & -C_2 & -C_1 & C_0 + 2C_1 + 2C_2 \end{bmatrix}.$$

Further, the inverse matrix  $\mathbf{C}^{-1}$  is compared with the coefficient matrix  $\mathbf{K}$  and the three partial capacitances are determined. Due to the high order of the equation systems, the analytical relations for  $C_0$ ,  $C_1$  and  $C_2$  are not presented here. Their values are directly obtained from numerical computations, e.g. Matlab®.

An approximation method for 5-conductor cables is to reduce the system order by 1 considering that two of the conductors are short-circuited, e.g. connected to ground. Thus the relations from 4-conductor cable can be applied with satisfactory results.

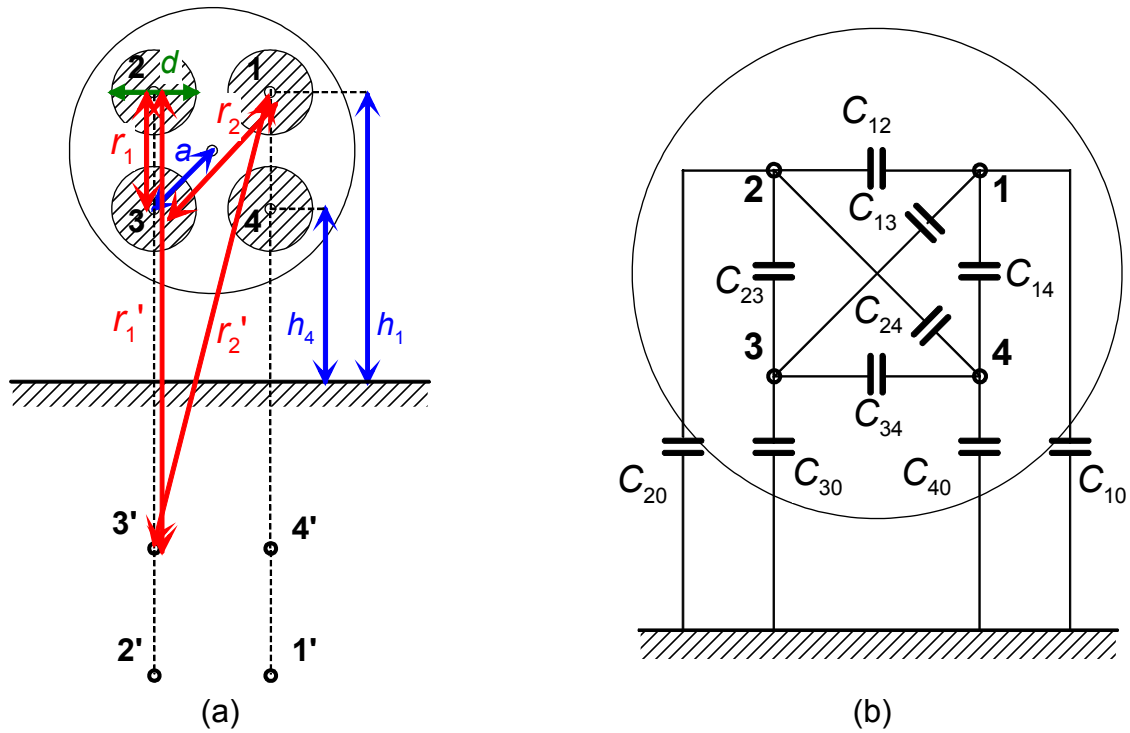


Figure 2.29: Geometrical configuration (a) and partial capacitances connection (b)

### 2.2.3.2 Unshielded cables

The unshielded cable is a different topology, where only a thick insulation jacket surrounds the conductors. Therefore, the equipotential surface is represented, in this case, by a distant surface (the earth). This leads to the condition distance conductor-ground  $\gg$  distance conductor-conductor, which in turn determines simplifications in the potentials equation systems. For example a **4-conductor unshielded cable** is considered (*PURWIL*, 6 mm<sup>2</sup>). The cable dimensions are: conductor diameter  $d = 3.18$  mm and distance  $a = 3.5$  mm. The geometrical configuration is shown in Figure 2.29 (a) and the partial capacitances in Figure 2.29 (b). The distances for the mirror-image method are:

$$r_1 = a\sqrt{2}, \quad r_1' = 2h_1 - a\sqrt{2}, \quad r_2 = 2a \quad \text{and} \quad r_2' = \sqrt{(2h_1 - a\sqrt{2})^2 + 2a^2}.$$

First, by assuming a distant equipotential surface,  $h_1$  and  $h_4$  can be approximated to be equal ( $h_1 \approx h_4 = h$ ). The ground potential is calculated as follows:

$$\varphi_0 = \frac{1}{2\pi\epsilon \cdot l} (Q_1 + Q_2 + Q_3 + Q_4) \ln \frac{h}{h} = 0.$$

This leads further to the system of equations similar to Eq. 2.36:

$$\varphi = \mathbf{K} \cdot \mathbf{Q}.$$

It can be noticed that, in this case, the coefficient matrix connects directly the potential matrix and the electric-charge matrix, having the following expression:

$$\mathbf{K} = \frac{1}{2\pi\epsilon \cdot l} \begin{bmatrix} x_1 & x_2 & x_3 & x_4 \\ x_2 & x_1 & x_4 & x_3 \\ x_3 & x_4 & x_1 & x_2 \\ x_4 & x_3 & x_2 & x_1 \end{bmatrix},$$

where the matrix elements are:

$$x_1 = \ln \frac{4h}{d}; \quad x_2 = \ln \frac{\sqrt{4h^2 + 2a^2}}{a\sqrt{2}} \approx \ln \frac{\sqrt{2} \cdot h}{a}; \quad x_3 = \ln \frac{\sqrt{(2h - a\sqrt{2})^2 + 2a^2}}{2a} \approx \ln \frac{h}{a};$$

$$x_4 = \ln \frac{2h - a\sqrt{2}}{a\sqrt{2}} \approx \ln \frac{\sqrt{2} \cdot h}{a}.$$

The number of partial capacitances is reduced to three when a symmetrical construction is considered: between conductors and ground  $C_0 = C_{10} = C_{20} = C_{30} = C_{40}$ , between two neighboring conductors  $C_1 = C_{12} = C_{23} = C_{34} = C_{14}$  and between two distant conductors  $C_2 = C_{13} = C_{24}$ . The partial capacitance matrix  $\mathbf{C}$  has a similar form like in the case of 4-conductor shielded cable. Comparing the inverse matrix  $\mathbf{C}^{-1}$  with the coefficient matrix  $\mathbf{K}$ , the partial capacitances are obtained. Due to the initial assumption  $h \gg a$ , the conductor-ground capacitance is very small and hence it can be neglected.

The obtained values are presented later in Appendix (subchapter 7.1), along with measurement and FEM results, for all types of discussed cable topologies.

### 2.2.3.3 Measurement of partial capacitances

In order to check the analytical results, several measurements at cables are conducted. An RLC-meter is used for capacitance, inductance and resistance measurements directly at the cable sample, whose length should be optimal in order to obtain good results. It is desired to carry out measurements for a wide frequency spectrum in order to get the parameters variation with frequency. But when the applied frequency is close or equal to the resonance frequency  $f_0$  of the cable, then the results are distorted. In [47] following types of cables are defined, with respect to phase constant  $\beta$ , wavelength  $\lambda$  and length  $l$ :

- $\lambda/2$  cables where  $\beta \cdot l = n \cdot \pi$ ,  $n = 1, 2, 3, \dots \Rightarrow l = \lambda \cdot n / 2$ ;
- $\lambda/4$  cables where  $\beta \cdot l = (2n - 1) \cdot \pi / 2$ ,  $n = 1, 2, 3, \dots \Rightarrow l = \lambda \cdot (2n - 1) / 4$ .

It can be noticed that the cables contain different resonance and anti-resonance points. The first resonant frequency occurs at  $n = 1$ . Knowing that:

$$\beta = \omega_0 \sqrt{L' C'}, \quad \text{Eq. 2.41}$$

and replacing Eq. 2.41 in  $\lambda/4$  cable condition, the first resonance frequency is obtained:

$$f_0 = 1/(4l \cdot \sqrt{L' C'}).$$

Here,  $L'$  and  $C'$  represent the phase values of inductance and capacitance per unit length. For example the 5-conductor shielded cable (*LAPP Classic 115CY*,  $2.5\text{mm}^2$ ) is

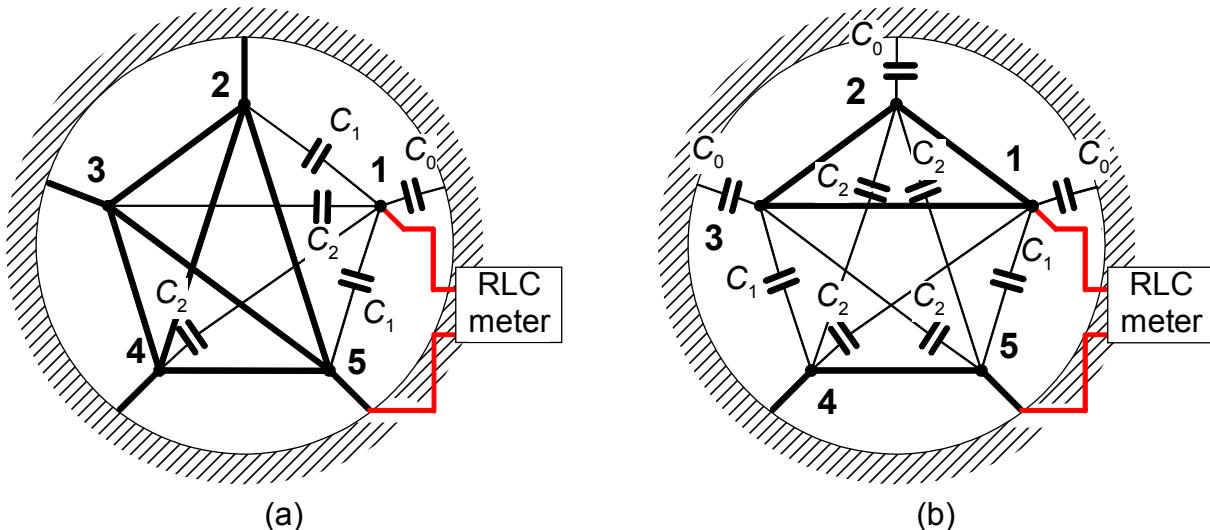
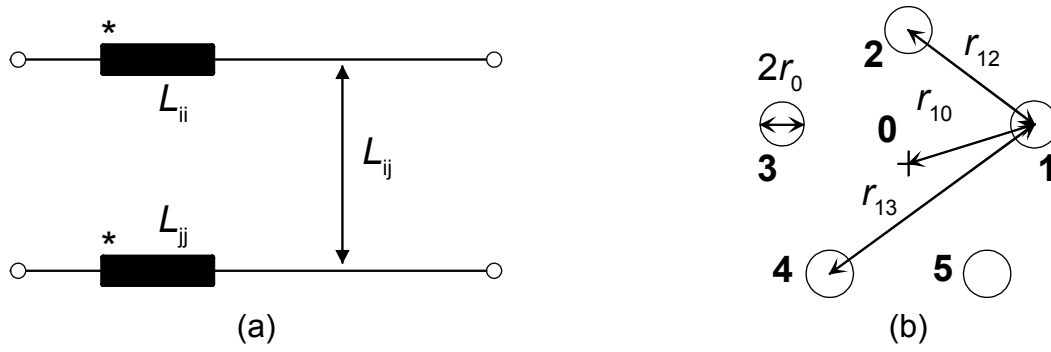


Figure 2.30: CM (a) and DM (b) configurations for capacitance measurements





**Figure 2.31: Self and mutual inductances (a); geometrical configuration (b) for inductance calculation**

considered.  $L'$  and  $C'$  are approximated to be:  $L' \approx 260$  nH/m and  $C' \approx 160$  pF/m, (details are offered in Appendix, section 7.1.1). Considering now two different cable lengths, the first resonance frequency is obtained:

- for  $l = 35$  m,  $f_0 \approx 1.1$  MHz;
- for  $l = 1$  m,  $f_0 \approx 38.7$  MHz.

It can be concluded that, using a cable length of 1 m the cable parameters can be measured up to a frequency of app 30 MHz without errors. By increasing the length of the cable sample, the measurable range decreases. On the other hand, a minimum cable length has to be considered, as the measurement device reaches its sensing limit. Further, samples of 1 m have been chosen to provide accurate results for all the cables.

The partial capacitances are impossible to measure individually without eliminating the effect of the others. Therefore, following configurations are used to determine the equivalent capacitances. They are calculated in parallel from the analytical values of partial capacitances and finally compared with the measured ones. First, the so-called common-mode (CM) configuration consists in measuring one conductor against all the others, which are short-circuited to the shield at the measuring side of the cable; see Figure 2.30 (a). It must be mentioned that, the remote cable end must be left opened to prevent circular currents. Thus, the equivalent capacitance  $C_A$  is obtained:

$$C_A = C_0 + 2C_1 + 2C_2.$$

Second, the differential mode (DM) connection is implemented when three conductors are short-circuited and the capacitance is measured between them and the remaining two connected to the shield (see Figure 2.30 (b)), obtaining the equivalent capacitance  $C_B$ :

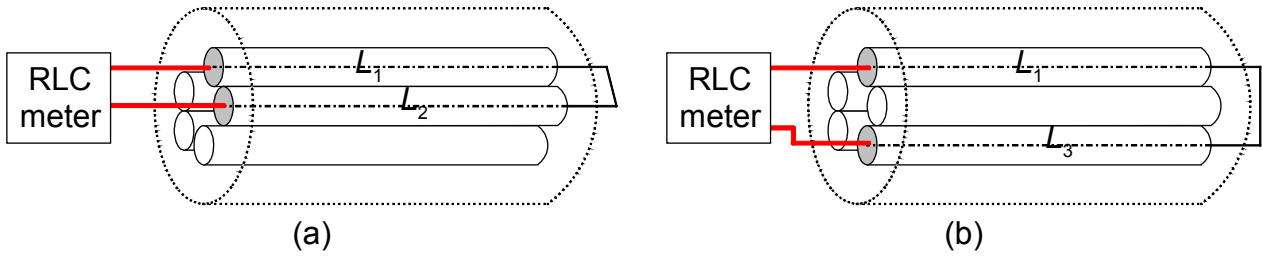
$$C_B = 3C_0 + 2C_1 + 4C_2.$$

The partial capacitances present a slight variation with frequency due to variable losses in the dielectric. Considering this changes to be small in comparison with the capacitance value, the capacitances can be assumed constant for the entire frequency spectrum.

## 2.2.4 Parameter identification - Inductances

Longitudinal inductances have an important role in modeling the cable, as they determine together with the capacitances the voltage wave propagation delay  $t_p = l \cdot \sqrt{L' \cdot C'}$  and hence, the wave oscillation period. Unlike capacitances, the inductance values depend strongly on frequency, mainly due to the skin and proximity effect, i.e. for low frequency the inductance value is high and decreases with increasing frequency.

In [50], an analytical method is proposed for the inductance calculation. For exemplification, the geometrical displacement of conductors from the 5-conductor shielded cable is used (*LAPP Classic 115CY*,  $2.5 \text{ mm}^2$ ). The inductance can be split into self-inductance  $L_{ii}$  of the conductor and mutual inductance between two conductors  $L_{ij}$ , like Figure 2.31 (a) shows. Here,  $i$  and  $j = 1 \dots 5$  represent the indices of the cable conductors. The geometric configuration, for calculating both inductances, is shown in Figure 2.31 (b).



**Figure 2.32: Phase inductance measurements for adjacent (a) and distant (b) conductors**

This inductances are calculated using the distances between conductors and the conductor diameter. First, the value for low frequencies is determined considering additionally the internal inductance (term  $\mu_r/4$ ):

$$L_{i\_LF} = \frac{\mu_0 \cdot l}{\pi} \left( \ln \frac{r_{i0}}{r_0} + \frac{\mu_r}{4} \right),$$

$$L_{ij\_LF} = \frac{\mu_0 \cdot l}{2\pi} \left( \ln \frac{r_{i0}^2}{r_0 r_{ij}} + \frac{\mu_r}{4} \right).$$
Eq. 2.42

The conductor radius is  $r_0$  and  $\mu_0$  stands for the magnetic permeability of the air. For high frequency, due to the skin effect, the current flows only at the surface of conductor. Therefore, the internal inductance is close to zero and the term  $\mu_r/4$  is neglected:

$$L_{i\_HF} = \frac{\mu_0 \cdot l}{\pi} \cdot \ln \frac{r_{i0}}{r_0},$$

$$L_{ij\_HF} = \frac{\mu_0 \cdot l}{2\pi} \cdot \ln \frac{r_{i0}^2}{r_0 r_{ij}}.$$
Eq. 2.43

The phase inductance is important for the calculation of the wave propagation delay and can be calculated from self and mutual inductance, see Eq. 2.42 and Eq. 2.43:

$$L_{ph\_LF} = 2(L_{i\_LF} - L_{ij\_LF}) = \frac{\mu_0 \cdot l}{\pi} \left( \ln \frac{r_{ij}}{r_0} + \frac{\mu_r}{4} \right),$$

$$L_{ph\_HF} = 2(L_{i\_HF} - L_{ij\_HF}) = \frac{\mu_0 \cdot l}{\pi} \cdot \ln \frac{r_{ij}}{r_0}.$$
Eq. 2.44

The cable inductances can be determined also by direct measurements at the cable sample. Actually the phase inductance is measured with the RLC meter as the self and mutual impedances cannot be separated from the cable bundle. The cable length should be short to prevent false measured values due to the resonance points. Moreover, due to the geometrical configuration of cables with more than 3 conductors, two types of phase inductances are distinguished: between two neighbor conductors and between two distant conductors. As it can be seen from Eq. 2.42 and Eq. 2.43, the influence of mutual inductance decreases with increasing the  $r_{ij}$  distance. This, in turn, determines larger phase inductances, like Eq. 2.44 shows. A measurement example is given for the 5-conductor shielded cable (*LAPP Classic 115CY*, 2.5 mm<sup>2</sup>). In Figure 2.32 (a) the measurement of the phase inductance between two adjacent conductors is shown, whereas the other case is illustrated in Figure 2.32 (b). The measured phase inductances have the following expressions:

$$L_A = 2(L_{11} - L_{12}), \quad L_B = 2(L_{11} - L_{13}).$$
Eq. 2.45

The opposite conductor ends are short-circuited to build the measurement loop. The remaining conductors are left unconnected at both ends to prevent any loop that might influence the measurements as an additional secondary winding.

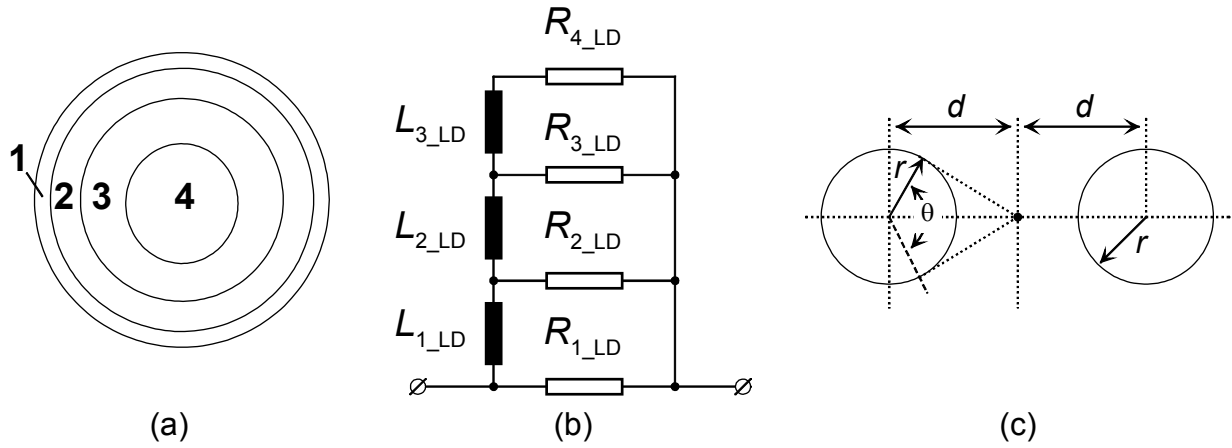


Figure 2.33: Conductor's cross-section (a), circuit for skin effect (b); proximity effect calculation (c)

### 2.2.5 Parameter identification - Resistances

The cable losses influence the wave attenuation along the cable and distort the ideal voltage waveform. Therefore, it is important to include the resistances to the cable model, as they are frequency dependent and increase dramatically with the frequency. The main reason for this increase represents the skin effect. Moreover, when conductors are close to each other in a cable bundle, the proximity effect determines a further increase of the resistance.

When high frequencies are used, the current tends to flow at the surface of conductor and a greater current density at the conductor surface (skin) than at its core is determined. The average depth, where current flows, is called skin depth. A consequence of the skin effect represents the increase of effective resistance and decrease of self-inductance. The main cause for the skin effect represents the eddy currents inside the conductor core, which increase with increasing frequency. The proximity effect determines the current in one conductor to be influenced by surrounding conductors and to flow on constrained regions at high frequencies. If the currents in two adjacent conductors flow in opposite directions, they will preferentially flow along the sides of the conductors that are facing each other. As a consequence, the effective resistance of the conductor increases.

In [51], a time-domain mathematical model is proposed to simulate the **skin effect**, which is based on dividing the conductor's cross-section into a finite number  $n$  of concentric sectors. A current density corresponds to each sector at a certain frequency. The cable cross-section is then modeled with a RL ladder circuit of  $n$  resistances and  $n-1$  inductances. A more practical approach is offered in [52], where the cable is divided in four concentric sections, like Figure 2.33 (a) shows. The corresponding RL ladder circuit is presented in Figure 2.33 (b). It consists of four resistances  $R_{i\_LD}$  for each sector and inductances  $L_{i\_LD}$  for couplings between each sector. In DC transmission (frequency 0), the inductances behave like short circuits and the equivalent resistance is given by the parallel connection of all four resistances. As the frequency increases so does the impedance of the coupling inductances. At high frequency they are seen as opened circuits and the equivalent resistance is given only by  $R_{1\_LD}$ .

Next, the calculation algorithm from [52] is presented. Following assumptions are taken considering the size of each concentric sector:

$$R_{4\_LD} < R_{3\_LD} < R_{2\_LD} < R_{1\_LD},$$

$$L_{3\_LD} > L_{2\_LD} > L_{1\_LD}.$$

Each sector is chosen so that  $R_{i\_LD}/R_{i+1\_LD} = k_R$ ,  $i = 1 \dots 3$ , i.e. the resistance values are set proportional. The first constraint is that the DC resistance of the ladder should be equal with the DC resistance of the conductor  $R_{DC}$ . The first resistance of the outer segment is

set  $R_{1\_LD} = \alpha_R \cdot R_{DC}$ , where  $\alpha_R$  represents the first proportionality constant. The equivalent DC resistance is calculated from the parallel connection of four resistances  $R_{i\_LD}$  and is given by the cubic function:

$$k_R^3 + k_R^2 + k_R + (1 - \alpha_R) = 0. \quad \text{Eq. 2.46}$$

Thus, for a given  $\alpha_R$ , the resistance ratio  $k_R$  is determined. Further, a similar proportionality is chosen also for inductances:  $L_{i\_LD}/L_{i+1\_LD} = k_L$ ,  $i = 1 \dots 2$ . The second constraint for ladder circuit refers to inductances: the low-frequency ladder inductance should be equal to the low-frequency internal inductance  $L_{LF}$  of the conductor. The first inductance is set  $L_{1\_LD} = L_{LF} / \alpha_L$ , where  $\alpha_L$  is the second proportionality constant. The inductance ratio  $k_L$  can be determined from Eq. 2.47, if the resistance factor  $k_R$  is known:

$$\left(\frac{1}{k_L}\right)^2 + \left(1 + \frac{1}{k_R}\right)^2 \frac{1}{k_L} + \left[\left(\frac{1}{k_R}\right)^2 + \frac{1}{k_R} + 1\right]^2 - \alpha_L \left\{ \left(1 + \frac{1}{k_R}\right) \left[\left(\frac{1}{k_R}\right)^2 + 1\right] \right\}^2 = 0. \quad \text{Eq. 2.47}$$

The proportionality factors  $\alpha_R$  and  $\alpha_L$  depend on the wire radius and the skin depth (which depends on frequency, permeability and conductivity). They are used for a curve fitting by comparing the analytical result with the measurements at a single conductor.

For the **proximity effect** the geometric arrangement from Figure 2.33 (c) is considered, where  $2d$  represents the distance between 2 conductors and  $r$  is the radius of the conductor. The angle  $\theta$  characterizes the dominant area, inside that the magnetic field between the 2 conductors will close, and can be calculated based on these distances using the following relation:

$$\frac{\theta}{2} = \arcsin\left(\sqrt{1 - \left(\frac{r}{d}\right)^2}\right). \quad \text{Eq. 2.48}$$

Further, the proportionality relation between the angle  $\theta$  and the complete angle  $2\pi$  ( $360^\circ$ ) can be expressed, using also Eq. 2.48, as follows:

$$\zeta = \frac{\theta}{2\pi} = \frac{1}{\pi} \cdot \arcsin\left(\sqrt{1 - \left(\frac{r}{d}\right)^2}\right), \quad \text{Eq. 2.49}$$

and, using this factor  $\zeta \in (0, 1)$ , the previous ladder circuit parameters are adjusted:

$$R'_{i\_LD} = R_{i\_LD} / \zeta; \quad L'_{j\_LD} = L_{j\_LD} / \zeta; \quad i = \overline{1,4} \text{ and } j = \overline{1,3}. \quad \text{Eq. 2.50}$$

The cable parameter values are summarized in Appendix, subchapter 7.1. For all the cable types, discussed in this work, the analytical and measured values are given in a table format. Moreover, parameters calculated with numerical methods, such as finite element simulations, are also offered. This work is a part of research collaboration between four institutes. Therefore, numerical parameter identification, using Finite Element Method (FEM) was implemented in a parallel research project [53] and will not be further detailed.

## 2.3 Motor simulation model

The electrical motor represents the third component of an electric drive. It converts the electric energy coming from the inverter to mechanical energy or reverse when it is operated as a generator. First converter-fed electric machines were the DC motors with brushes. They became obsolete with the time because of large dimensions and maintenance and were replaced by induction motors. From these, the squirrel cage induction machine is mostly used in industry due to its low cost and relative high efficiency. Unlike DC-motors, the induction motors present a three-phase stator winding which can be fed directly from grid or using electric converters to obtain variable torque and speed. An alternative to induction motors represents the permanent magnet synchronous motors (PMSM). Their cost is higher compared to induction motors, because the rotor flux is produced by the permanent magnets placed on the rotor. However, the PMSMs are easier to control and show a higher efficiency. Further, induction motors will be analyzed.

Simulation models for induction motors, based on the stator and rotor equations, are well known in literature. They are used to design and test modulation techniques and/or different control methods. But, these models are valid only for the fundamental frequency range (up to few hundred Hz). To analyze the HF phenomena (frequency range around 1 MHz), models based on the parasitic elements should be considered. Of great importance is the simulation of the motor input impedance  $Z_L$ . This impedance together with the cable impedance  $Z_C$  determines the reflection coefficient at the motor cable end  $K_L$  and the voltage wave behavior on the cable (Eq. 2.19). The motor input capacitance plays an important role for the wave oscillation period on the cable, as it alters the wave propagation speed. Measurements and simulations will be discussed in section 3.2.3.

Similar to the IGBT case, there are two major approaches when modeling an electric motor: based on the physical dimensions and behavioral model or equivalent circuit. The main part of the HF motor model represents the stator winding together with the capacitive coupling to the motor case. The inductive coupling to rotor is large and, therefore, can be neglected for HF simulations.

### 2.3.1 Distributed parameter model

The distributed parameter model of the motor [34] is based on traveling-wave theory. Similar to cables, the motor windings are modeled by connecting more  $\Gamma$  circuits (see Figure 2.34). The traveling wave excites each  $\Gamma$  section and determines distributed parasitic effects. The number of  $\Gamma$  sections equals the number of turns per phase  $N_s$ . Besides the longitudinal resistance  $R_i$  and inductance  $L_i$ , the capacitive coupling to the

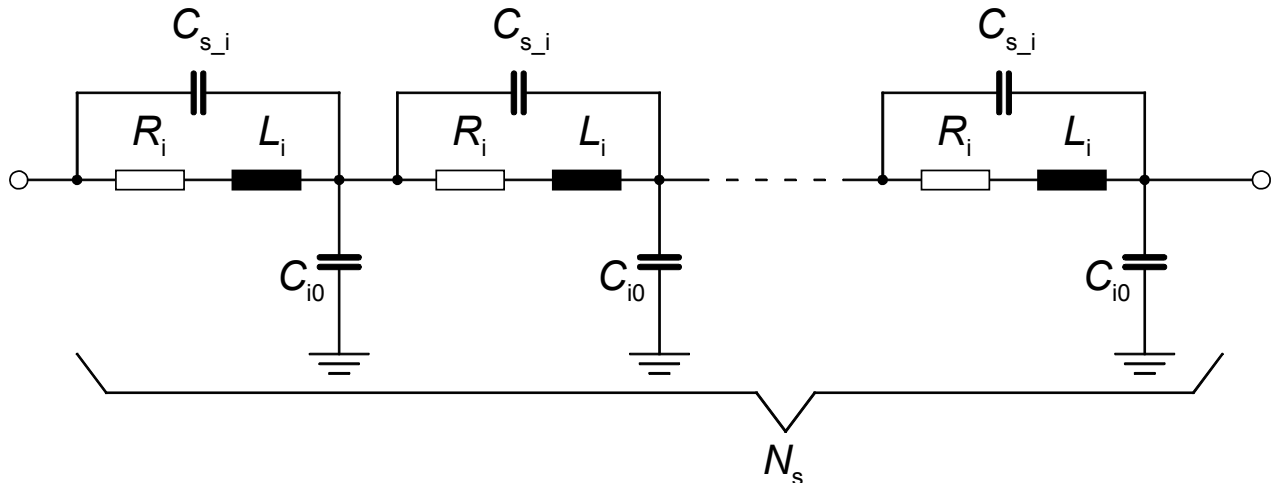


Figure 2.34: Per phase lumped parameter circuit of stator windings

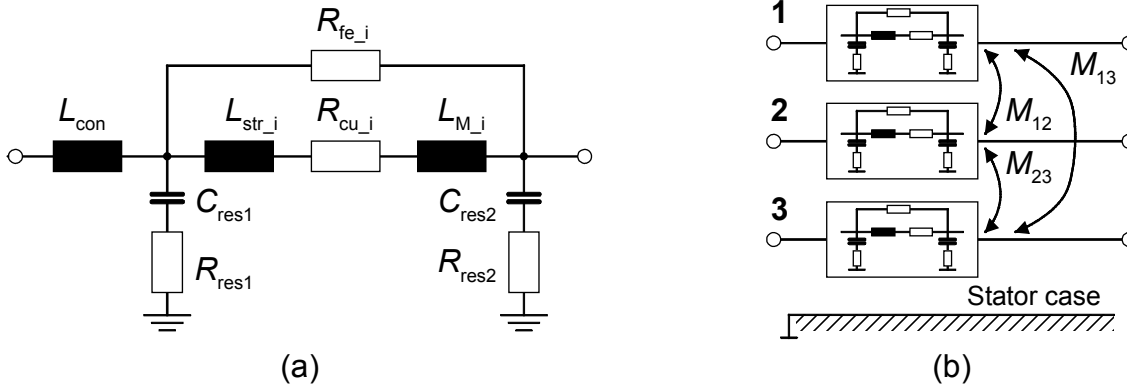


Figure 2.35: Per phase motor equivalent circuit (a) and complete motor model (b)

stator case  $C_{i0}$  is included, where  $i = 1 \dots 3$  represents the phase number. Moreover,  $C_{s\_i}$  models the capacitive coupling between two turns.

This type of motor models is complex, but simulates the voltage distribution across the windings with the help of the inter-turn capacitance  $C_{s\_i}$ , starting from the motor-input terminals. The distributed-parameter model can be parameterized only if the motor physical properties and the internal design are known. In a similar way as for cables, the capacitances between stator coil and case or between two stator coils can be calculated, analytically or using numerical methods, only if the geometrical structure and the material properties are known. Thus, such models are useful to implement in the design stage of the electrical motors or for new prototypes [17]. The model parameters can be determined by means of finite element simulations, knowing the desired motor layout and following two steps: first, the electric field is calculated, using static analysis, which leads further to the determination of capacitances and second, inductances and resistances are determined from magnetic field and losses calculations using the harmonic AC analysis.

If the internal dimensions and properties are not available for a user, than this model type is unpractical. Therefore, a similar approach similar to the IGBT case has to be adopted, i.e. the motor should be modeled with an equivalent circuit, which can be easily parameterized from direct measurements at the motor terminals.

### 2.3.2 Equivalent circuit model

To model the motor with an equivalent circuit, only the motor behavior should be known. In this way, the model is regarded as a black box and the transfer characteristic is simulated using circuit elements. The model parameterization is based on the direct measurements of the input impedance at the motor terminals [36].

In Figure 2.35 (a), the equivalent circuit per one phase of the machine is shown. The winding is represented using the self-inductance and the copper resistance  $R_{cu\_i}$ . The self-inductance is coupled only to the other phase inductances of the stator. To represent it better, the winding inductance is separated into a fully coupled part  $L_{M\_i}$  and a stray inductance  $L_{str\_i}$ .  $R_{fe\_i}$  simulates the iron losses of the motor phase  $i$ . There are two capacitances coupling the stator winding to the case,  $C_{res1}$  and  $C_{res2}$ , each corresponding

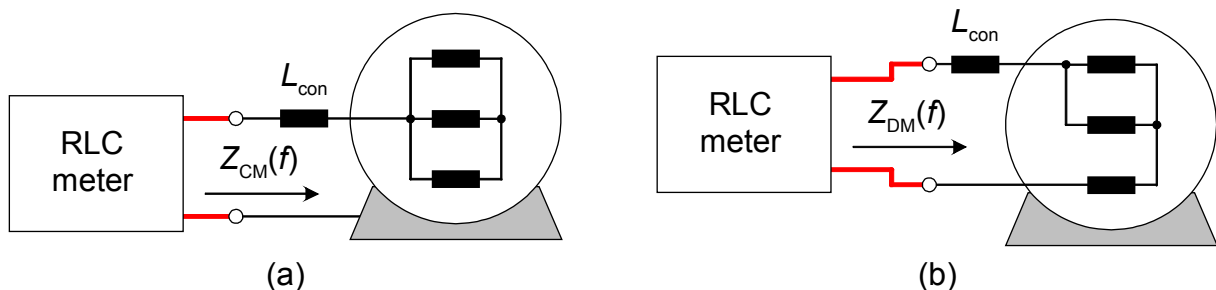


Figure 2.36: CM (a) and DM (b) measurement configurations

to different resonant points. Moreover, the damping of the input impedance in the two resonant points is simulated using  $R_{\text{res}1}$  and  $R_{\text{res}2}$ . Finally, connecting the three phases in parallel, the motor model is built, like in Figure 2.35 (b) shown. The inductive coupling is modeled using the mutual inductances  $M_{ij}$ . At the opposite side, the phases are short-circuited together to obtain the neutral point. The motor case is connected to ground.

There are limitations of this model type, as the voltage distribution across the winding cannot be simulated. To include additional parasitic effects, like bearing currents, this model can be completed with bearings, using equivalent circuit models for them [54].

### 2.3.3 Parameter identification

The model parameters can be determined from input-impedance measurements at the motor terminals. There are two measurement configurations: common mode (CM) and differential mode (DM), shown in Figure 2.36. For the CM configuration, the measurement is done between all phases connected together and the motor case. In the DM case, the impedance is measured between one phase and the remaining two phases, which are short-circuited.

For example, a 5-kW squirrel-cage induction machine is considered. In the Figure 2.37, the measured and simulated amplitudes and phases are plotted for a wide range of frequency, considering both the CM and DM configurations. To calculate the parameters, following algorithm is used [36]:

**Step 1.** For Common-Mode configuration, the circuit from Figure 2.38 (a) is considered. Generally, the measured impedance presents a capacitive behavior for the entire frequency spectrum. At high frequencies (region around point 1 in Figure 2.37 (a),

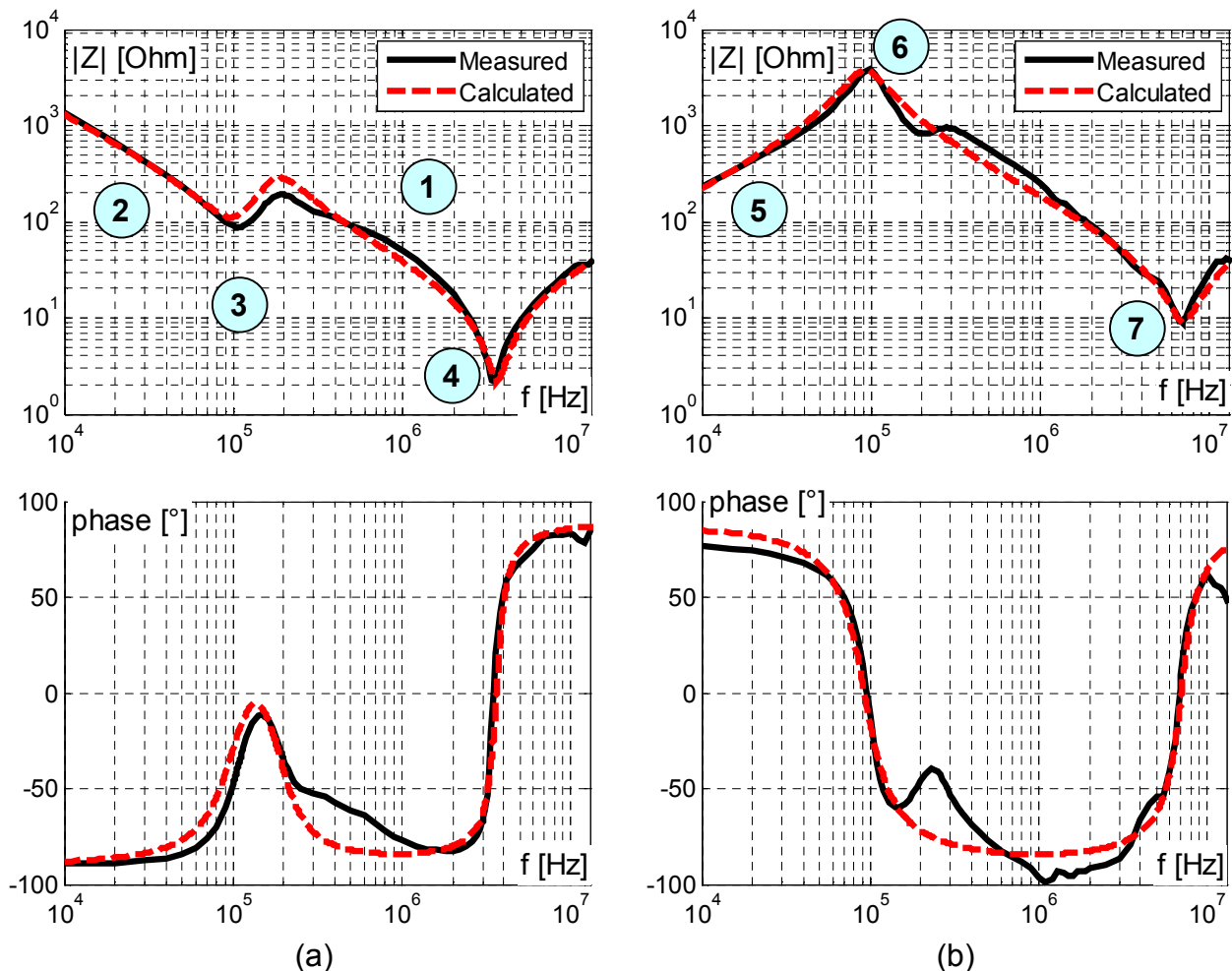


Figure 2.37: Impedance amplitude and phase frequency characteristic for CM (a) and DM (b)

between 300 kHz and 2 MHz), the common-mode inductance  $L_{CM}$  behaves like an open circuit (high impedance). Therefore, a capacitive behavior (phase closed to  $-90^\circ$ ) is noticed and the impedance is dominated only by capacitance  $C_{res1}$ :

$$C_{res1} = \frac{1}{3} \cdot \frac{1}{2\pi \cdot f|_{pt.1} \cdot |Z_{CM}|_{pt.1}}. \quad \text{Eq. 2.51}$$

At lower frequencies (region around point 2 in Figure 2.37 (a), below 70 kHz), the common-mode impedance  $j\omega L_{CM}$  is small and can be neglected. This determines a capacitive behavior of the impedance (parallel connection between  $C_{res1}$  and  $C_{res2}$ ):

$$C_{tot} = \frac{1}{3}C_{res1} + \frac{1}{3}C_{res2} = \frac{1}{3} \cdot \frac{1}{2\pi \cdot f|_{pt.2} \cdot |Z_{CM}|_{pt.2}}. \quad \text{Eq. 2.52}$$

Knowing the values for  $C_{tot}$  and  $C_{res1}$ , the capacitance  $C_{res2}$  can be determined:

$$C_{res2} = 3 \cdot (C_{tot} - \frac{1}{3}C_{res1}).$$

Between both regions, the first resonant point is observed (point 3 in Figure 2.37 (a) at approximately 100 kHz). Here, the effect of  $L_{CM}$  is noticeable. For a frequency interval after the resonant point, the modulus of the input impedance tends to increase whereas the phase shifts towards  $+90^\circ$ . An anti-resonance peak follows and the impedance modulus starts to decrease again. The phase decreases back towards  $-90^\circ$ . The common-mode inductance  $L_{CM}$  can be calculated at first resonance point using the resonance frequency:

$$\omega_{0\_pt.3} = \frac{1}{\sqrt{L_{CM} \cdot 3C_{res2}}} = 2\pi f_{0\_pt.3} \Rightarrow L_{CM} = \frac{1}{12\pi^2 \cdot f_{0\_pt.3}^2 \cdot C_{res2}}, \quad \text{Eq. 2.53}$$

where only  $C_{res2}$  contributes to the resonance. Considering the minimum impedance modulus in this point:

$$|Z_{CM}|_{min|_{pt.3}} = 87.9 \Omega \text{ @ } f_{0|_{pt.3}} = 107 \text{ kHz},$$

the damping factor  $R_{res2}$  can be calculated:

$$R_{res2} \approx 3 \cdot |Z_{CM}|_{min|_{pt.3}}.$$

If the effect of  $R_{fe\_i}$  is considered not to be negligible, than the expression for  $R_{res2}$  becomes (see Figure 2.38 (a)) [36]:

$$R_{res2} = 3 \cdot |Z_{CM}|_{min|_{pt.3}} - \frac{9R_{fe\_i}(2\pi \cdot f_{0\_pt.3} \cdot L_{CM})^2}{R_{fe\_i}^2 + 36\pi^2 \cdot f_{0\_pt.3}^2 \cdot L_{CM}^2}.$$

**Step 2.** The *Differential-Mode* configuration is represented in Figure 2.38 (b) by the simplified three-phase circuit. The input-impedance measurement presents, in this case, an inductive behavior (the modulus is increasing while the phase is around  $+90^\circ$ ) up to a resonance frequency, see point 5 in Figure 2.37. In this region (below app. 70 kHz) the effect of DM equivalent inductance  $L_{DM}$  is dominant. Choosing a point on the modulus slope, the value can be easily calculated:

$$L_{DM} = \frac{|Z_{DM}|_{pt.5}}{2\pi \cdot f|_{pt.5}}. \quad \text{Eq. 2.54}$$

A value much larger than  $L_{CM}$  is obtained for  $L_{DM}$  (see Table 7.8 in section 7.2.1 (Appendix)). Thus, coupling effects between the self-inductances  $L_{s\_i}$  must be considered. The first anti-resonance, from point 6, changes the behavior from inductive to capacitive, i.e. the impedance modulus starts to decrease and the phase shifts towards  $-90^\circ$ . At point 6, the impedances of the phase-to-ground capacitances  $C_{res1}$  and  $C_{res2}$  are assumed to be large. Therefore, only  $R_{fe\_i}$ , connected in parallel to  $L_{s\_i}$  (Figure 2.35 (a)), is considered responsible for the damping of the resonance and the following expression is valid:



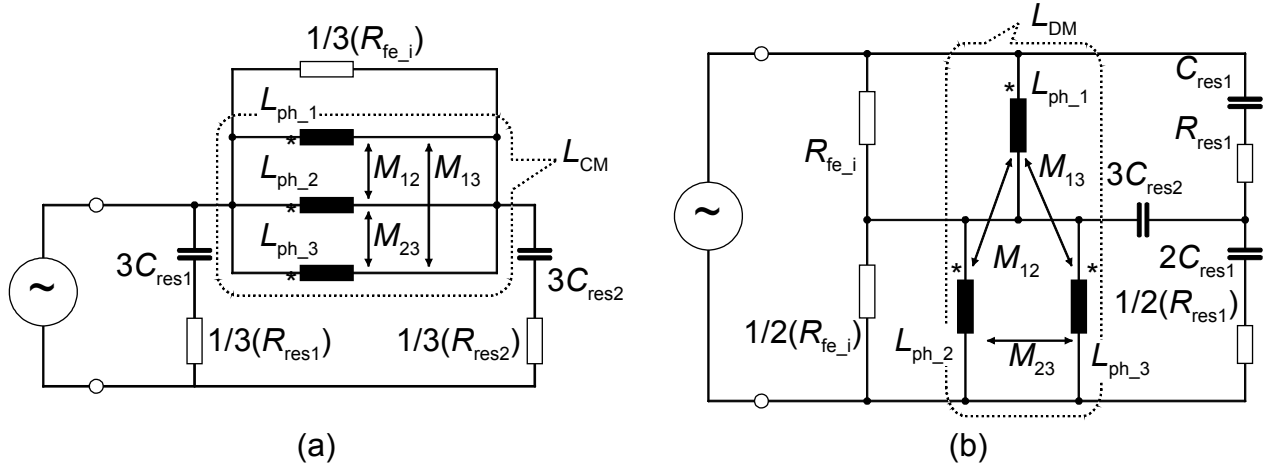


Figure 2.38: Simplified three-phase circuit for CM (a) and DM (b) measurements

$$R_{fe\_i} \approx \frac{2}{3} \cdot |Z_{DM}|_{\max}|_{pt.6},$$

Eq. 2.55

where  $|Z_{DM}|_{\max}|_{pt.6} = 3.78 \text{ k}\Omega @ f_0|_{pt.6} = 98 \text{ kHz}$ .

For high frequencies, the parasitic effects of the cable connectors cannot be neglected. The stray inductance  $L_{con}$  of the connectors contributes to the second resonance at point 7, see Figure 2.36. A similar relation like Eq. 2.53 is used here, but the resonance is determined in this case by the product of  $L_{con}$  and  $C_{res2}$ :

$$L_{con} = \frac{3}{16\pi^2 \cdot f_{0\_pt.7}^2 \cdot C_{res1}}.$$

The resonance damping in this point is simulated using  $R_{res1}$ , which can be expressed in a similar way like  $R_{fe\_i}$ :

$$R_{res1} = \frac{2}{3} \cdot |Z_{DM}|_{\min}|_{pt.7},$$

where  $|Z_{DM}|_{\min}|_{pt.7} = 9.09 \text{ }\Omega @ f_0|_{pt.7} = 6.9 \text{ MHz}$ .

**Step 3.** The self-inductance  $L_{s\_i}$  and the mutual inductance  $M_{ij}$  can be calculated out of common-mode and differential-mode inductances. From Figure 2.38, we obtain the following relations:

$$L_{CM} = \frac{1}{3}(L_{s\_i} + M_{ij})$$

$$L_{DM} = \frac{3}{2}(L_{s\_i} + M_{ij})$$

Eq. 2.56

and, solving Eq. 2.56, we get:

$$L_{s\_i} = L_{CM} + \frac{4}{9}L_{DM}$$

$$M_{ij} = L_{CM} - \frac{2}{9}L_{DM}$$

Further, the stray inductance  $L_{str\_i}$  and the coupling inductance  $L_M$  are determined, using following relations:

$$L_{str\_i} = L_{s\_i} - |M_{ij}|$$

$$L_M = |M_{ij}|$$

Finally, the winding resistance  $R_{cu\_i}$  is approximated with the copper resistance of the winding conductor at 0 Hz. Usually this resistance does not exceed 5  $\Omega$ . Table 7.8 from section 7.2.1 (Appendix) summarizes the obtained parameter values for the BBC 5-kW induction motor. The measurements for the input impedance were presented in Figure 2.37. The calculated parameter values are used to implement the equivalent circuit from Figure 2.35 (a) for one phase. By connecting three equivalent circuits, as shown in Figure 2.35 (b), the input impedance is calculated and its frequency characteristic plotted in Figure 2.37 (dashed curve). A good approximation of measured values is obtained using the considered simplifications.

A second induction machine (Siemens 4-kW), for the same power range, was analyzed and the HF model parameterized using the same methods presented previously. The simulation model parameters and the input-impedance measurements are presented in section 7.2.2 (Appendix).

### 3 Comparisons between measurements and simulations

#### 3.1 Test setup

To validate the simulation results, an inverter was designed and realized. Commercially available inverters are usually compact and realized in a single unit. There is no access to measure internal quantities, like collector current, for a single IGBT. With commercially available inverters, the user has only the option to change the switching frequency in some discrete range but not the switching profile. The quantities at the IGBT gate connections are not accessible. Therefore, the design and realization of a custom inverter is necessary for further investigations.

##### 3.1.1 Inverter hardware

First, the IGBT module [43], presented in subchapter 2.1, was used to design the inverter. Figure 3.1 presents the electric schematic and a picture of the real module. The red connections are realized externally on the inverter PCB. The advantage is that the lower legs are not connected with each other. This facilitates the connection of a shunt resistor at the terminal “ET”. Thus, the current  $I_{C6}$ , which flows only through the lower IGBT from the third leg, can be measured. Another criterion for choosing the IGBT module is the power level. A 5 kW-rated power induction motor has to be driven. The rated power of inverter is chosen always higher than of the drive to allow a safe margin operation.

The inverter is designed and implemented on a Printed Circuit Board (PCB), as Figure 3.2 shows. The inverter bridge and the diode rectifier are placed on the same board. They are connected and fixed on the bottom side to the heat sink. To drive the IGBT module, a 6-pack Gate Drive Unit (GDU) is used. The currents are measured at the inverter output for control purposes using magneto-resistive sensors. The output of the sensors is then adapted using operational amplifiers and sent to the module interface board. The shunt  $R_{shunt}$ , used to measure the collector current of a single IGBT, is shown in Figure 3.2.

The DC-link capacitors are placed between the diode rectifier and the inverter bridge. Due to the unconventional pin layout of the IGBT module, the DC-link bus from Figure 3.3 was designed. The positive DC-link connection corresponds to the top layer and the negative to the bottom layer. Most important parasitic elements of the DC-link bus are the stray inductances as they influence the switching behavior. They can be determined either by direct measurements or from FEM calculations [45]. Analytical relations are difficult to use due to the complicated geometry structure. The different values for the DC-link stray inductances are obtained for different lengths of the conduction paths, like Figure 3.3 shows. For example, the biggest value is obtained for the stray inductance  $L_{loop2}$ , as the

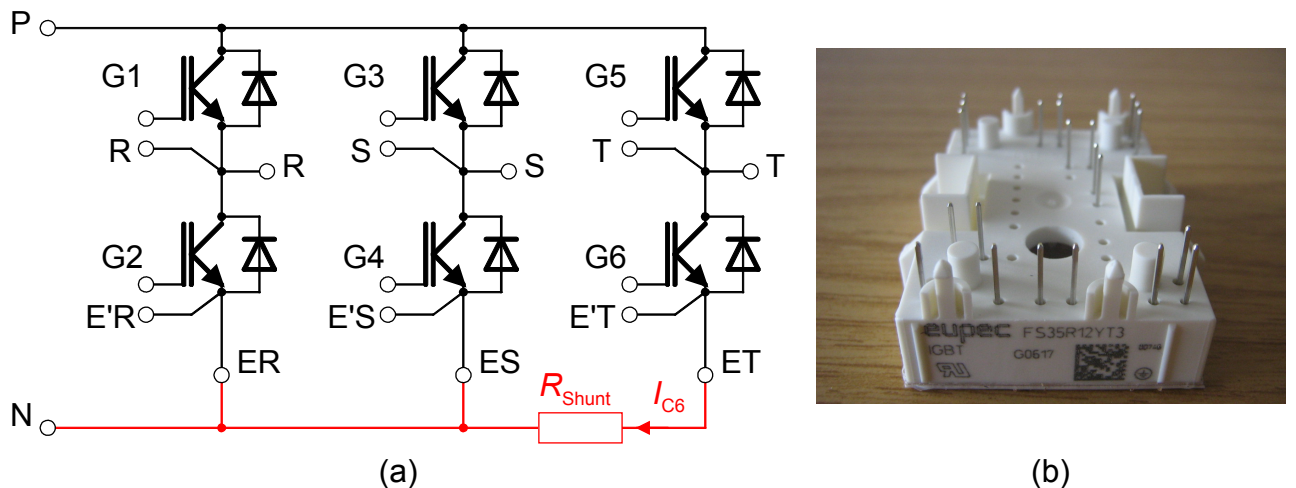


Figure 3.1: IGBT module electric schematic (a) and photo (b)

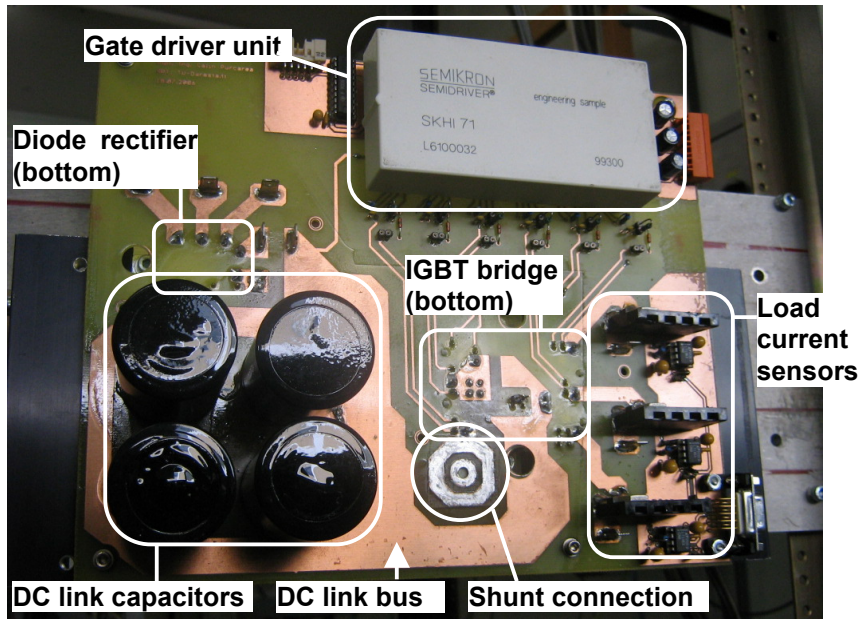


Figure 3.2: Inverter printed circuit board (PCB)

corresponding path is the largest; see Figure 3.3 (b). The measured and calculated values are summarized in Table 3.1. Both measurements and calculation results are considered at high frequencies, i. e. around 1 MHz. Because the individual inductances cannot be measured, following loop inductances are approximated:

$$L_{\text{loop1}} = L_{\sigma\_DC\text{-link1}} + L_{\sigma\_DC\text{-link2}},$$

$$L_{\text{loop2}} = L_{\sigma\_DC\text{-link3}} + L_{\sigma\_DC\text{-link4}}.$$

The effects of the mutual inductances inside the loops are already included in the stray inductances  $L_{\sigma\_DC\text{-link1}\div4}$ .

### 3.1.2 Current measurement shunt

To measure the collector current, a coaxial shunt topology was chosen. In [25], a comparison between different current measurement devices, like Pearson current sensor, Rogowski coil, current transformers, etc., is offered. The coaxial shunt was found to be a good solution due to its advantages: high precision, no measurement dead time and theoretical very high bandwidth, limited only by construction. In Figure 3.4 the schematic of such coaxial shunt is presented together with a photo. It can be noticed that the total inductance is kept low using a sandwich structure, where currents are flowing in opposite

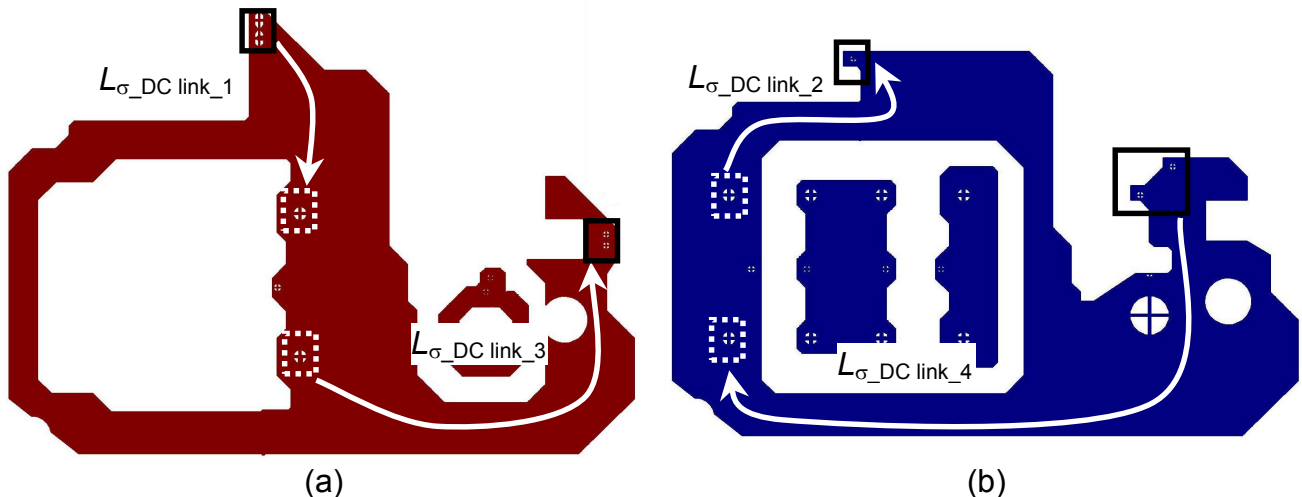


Figure 3.3: Figure 3.3 Top (a) and bottom (b) layers of DC-link bus

directions (like for DC-link bus), i.e. the magnetic fields from both current paths will cancel each other. At our department, coaxial shunts were developed for high-power modules with screw connections [25]. Such a module was adapted for low-power modules by increasing the length. The screw mounting part is kept (Figure 3.4 (a)) and the shunt is fixed directly to the PCB using adapted copper surfaces (Figure 3.2). The current flows in the axial direction through a thin Manganin<sup>®</sup> sheet. This material has good temperature stability. The voltage is picked up at both ends of Manganin<sup>®</sup> sheet and sent to oscilloscope by a BNC female connector.

**Table 3.1: Calculated vs. measured DC-link bus stray inductances**

	Calculated	Measured
$L_{loop1}$ / nH	64.07	65.4
$L_{loop2}$ / nH	87.17	83.9

The main disadvantage is that the current measurement is not isolated from the measurement devices, such as oscilloscopes. For safety reasons, the housing of measurement devices operated by humans are mandatory connected to protective earth (PE). If the DC-link voltage is supplied from an isolated power supply, than the negative DC-link bus can be connected to PE and no potential separation is required. But, in industrial converters the negative DC-link bus is floating at  $-300$  V with respect to ground due to the diode bridge rectifier. Therefore, it is mandatory to separate the potentials. In this case, the high-potential part is separated using differential amplifiers.

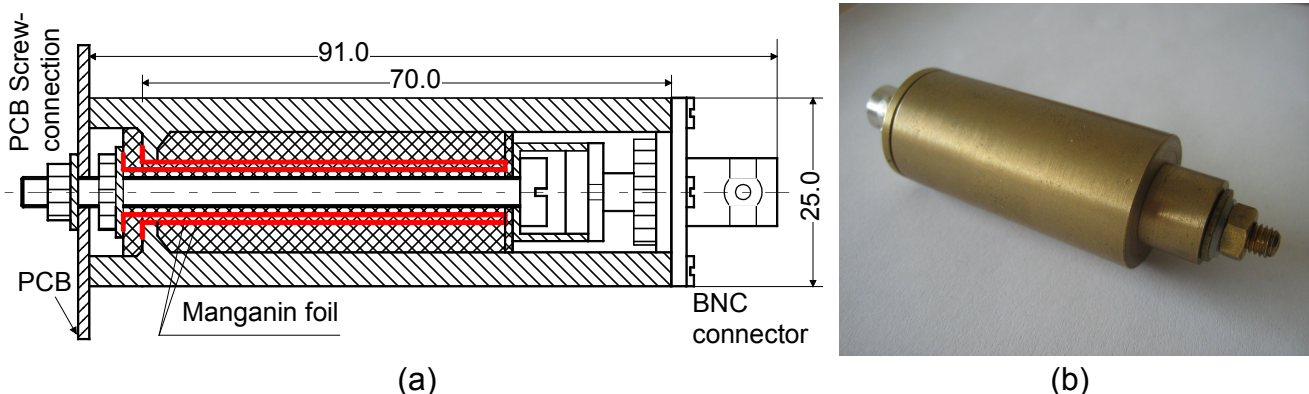
Special attention is required when choosing the bandwidth of differential amplifiers. The fastest transient of the IGBT represents the current rise time  $t_r$  [43]: around 20 ns in worst case. Therefore a differential amplifier with bandwidth of 100 MHz is considered to be sufficient. Moreover, the fastest voltage transient is around 100 ns, which is far below the cutoff frequency of the differential amplifier.

### 3.1.3 Inverter command and control

To control the switching instants of the inverter, a system based on a PC and a real-time communication via an inverter bus is used [55]. Therefore, an additional hardware is needed to realize the interfacing between PC and inverter. This device, developed at our department and called “Antrieb Module Interface” (AMI) [55], supervises and controls the switching state of the inverter while communicating with the PC. The two main tasks are:

- generate the switching commands for inverter GDU, based on switching time intervals obtained from PC;
- read the load currents, transform them from analog to digital values and transfer the digital values to PC.

The AMI board, shown in Figure 3.5, is divided in two main parts: analog and digital. The analog part is located in the middle and consists of two stages of signal adaptation using operational amplifiers. The signals from the current sensors are amplified and filtered again before A/D conversion. On the left side, the measured currents are compared with adjustable references to detect over-currents in inverter.



**Figure 3.4: Coaxial measurement shunt: schematic (a) and photo (b)**



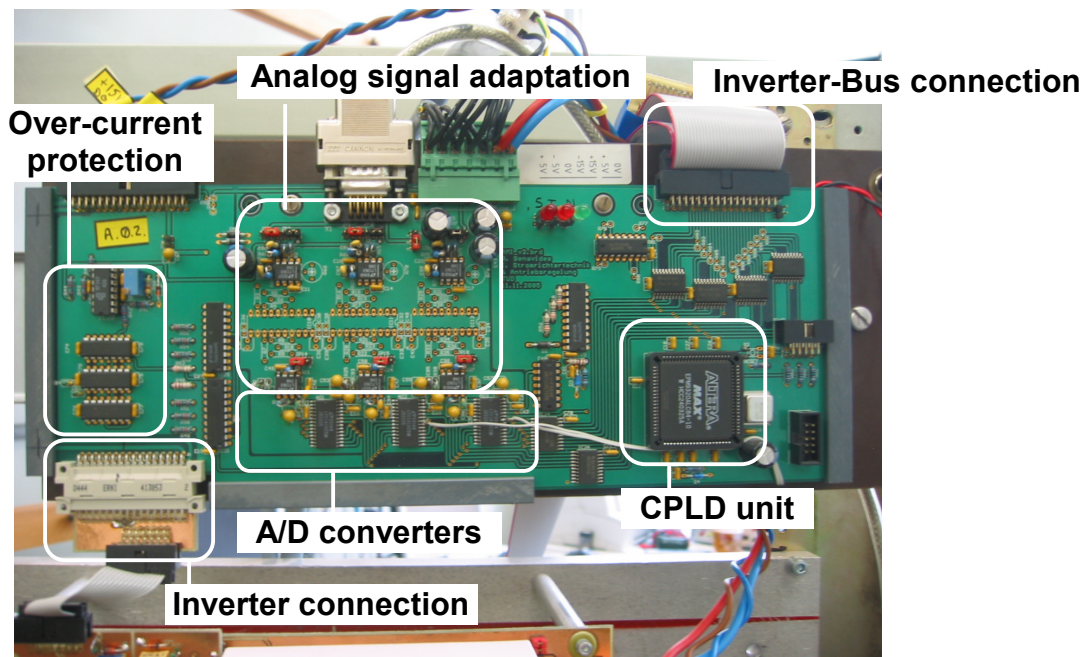


Figure 3.5: Components of the AMI board

The main device from the digital part represents the CPLD logic unit. Here, the logic state machine is implemented, which realizes following tasks: communication with PC, control of A/D converters and monitoring activity with inverter shutdown in case of errors (communication or over-current).

The AMI – PC communication is based on a bus system, also called ‘Inverter-Bus’. 16 parallel signals (twisted pairs) are used for communication (RS485 standard). Out of these 16 signals, 4 are control signals and the rest 12 are used for data transmission [55]. At the inverter side, the six switching signals coming from CPLD unit are buffered and sent to the gate drive unit (GDU). As already mentioned, the currents are digitalized using 12-bit A/D converters. When the conversion is ready and the communication protocol requests a transfer, the current values are placed directly on the inverter bus.

At the PC side of the Inverter-Bus, an additional board, called ‘Fahrzeug-Interface’ (FZI), is responsible for communication control with the AMI board; see Figure 3.6 (a). The state machine is implemented in a FPGA logic unit, which interfaces the Inverter-Bus with

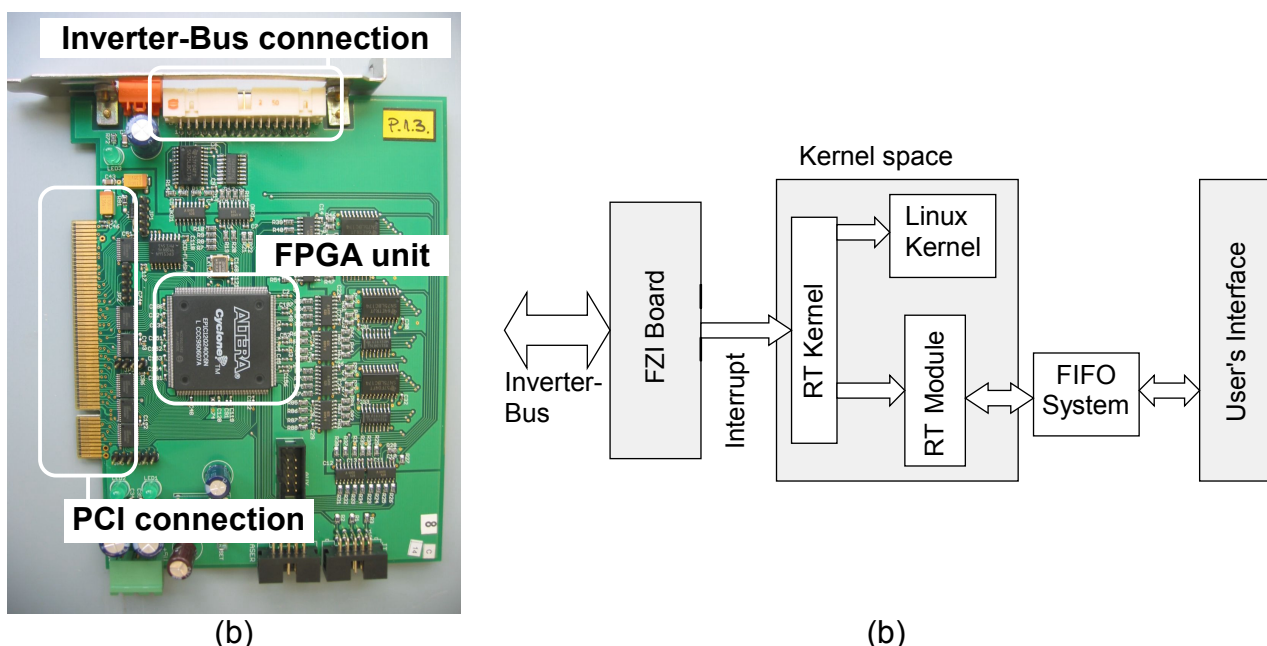
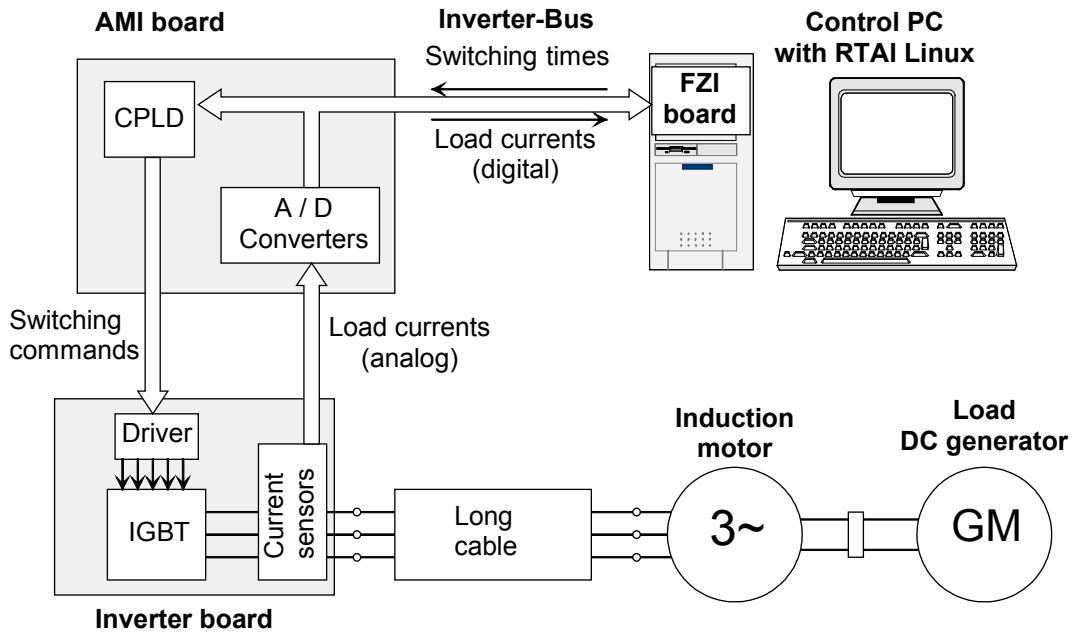


Figure 3.6: FZI Board (a) and real time control structure (b)



**Figure 3.7: Control system architecture**

peripheral PCI bus system of the computer. Here, the Bus-Master is implemented allowing the real-time communication with more AMI boards. On the same Inverter-Bus, a single FZI can address up to 18 AMI boards in a single control cycle. The control cycle corresponds to the half of the switching interval, i.e.  $100\ \mu\text{s}$ . The electric connection to the AMI board is isolated by optocouplers to avoid ground loops or EMI problems [56].

The control algorithm of the inverter is implemented on PC. In order to work with small control cycles, like  $100\ \mu\text{s}$ , a real-time operation system (RT-OS) has to be used. In this case a Linux distribution is chosen, where the additional module for Real Time Application Interface (RTAI) makes this OS real time capable. In Figure 3.6 (b) the simplified schematic is shown. The RT kernel behaves like a buffer layer between the Linux kernel and the FZI hardware. A hardware interrupt is generated from the FZI and is detected by the RT kernel using the Interrupt Service Routine (ISR). In the time interval between each ISR call, the other control tasks are executed, using the real time module (RTM). Because the RTM is situated in the kernel space, a FIFO stack communication system is implemented to exchange data between RTM and Graphic User Interface (GUI) [56]. Two FIFO stacks are used here: one to get the data about the process necessary for the control algorithm from RTM to GUI, e.g. measured currents or voltages; the other to send commands to RTM from GUI, e.g. start / stop the control or set different parameters. Thus, a full flexibility is offered to user although the RTM is not accessible.

To conclude, Figure 3.7 shows the entire control system configuration. The control program runs under real time operation system on the control PC. Each half of switching cycle (control cycle is  $100\ \mu\text{s}$ ) the control program (RTM part) gives the switching times to the FZI board, which sends them further to the AMI board via the Inverter-Bus. Based on the received switching times, the modulator from AMI board generates the switching signals for inverter. Next step is converting the load currents to digital values and sending them back to the RT Module (located in the control PC) via Inverter-Bus and FZI. The communication cycle uses  $5\ \mu\text{s}$  from entire control cycle. The rest remains for execution of the control functions and operations [55].

### 3.2 Simulations and measurements

In order to check the reliability of the designed simulation models, comparisons with measurements at the real setup are necessary. Further, each part of the ASD, i.e. inverter, cable and motor, will be treated separately to understand better the individual characteristics and limitations of the chosen model types.

#### 3.2.1 Inverter simulations and measurements

First, a buck-converter topology is used to test the switching transients of the IGBT. The setup configuration from Figure 3.8 is used, where an inductive load is directly connected between the positive DC-link bus and the 3<sup>rd</sup> phase inverter output. The lower IGBT from the 3<sup>rd</sup> leg is investigated, considering also the stray elements of the DC link. A short train of pulses is used to switch the IGBT. Because the load is inductive, special attention in selecting the switching intervals must be taken not to exceed the current limit. Here, four pulses are used to obtain the turn-on and turn-off transients for different levels of the collector current, see Figure 3.8 bottom right. In each case, three main quantities are measured:  $V_{CE}$ ,  $I_C$  and  $V_{GE}$ . Further, important parameters like voltage rise or fall time ( $t_r$  or  $t_f$ ) for  $V_{CE}$ , current slopes for  $I_C$  and collector-emitter charges during transitions are

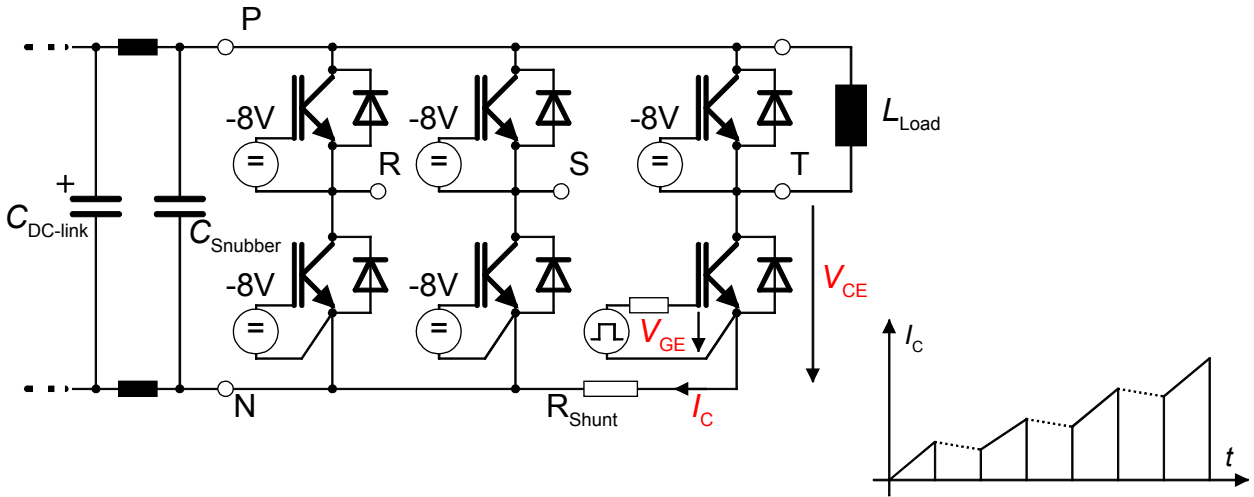
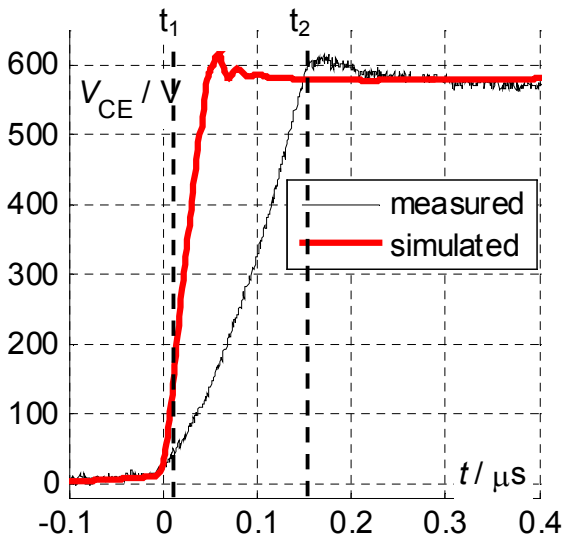
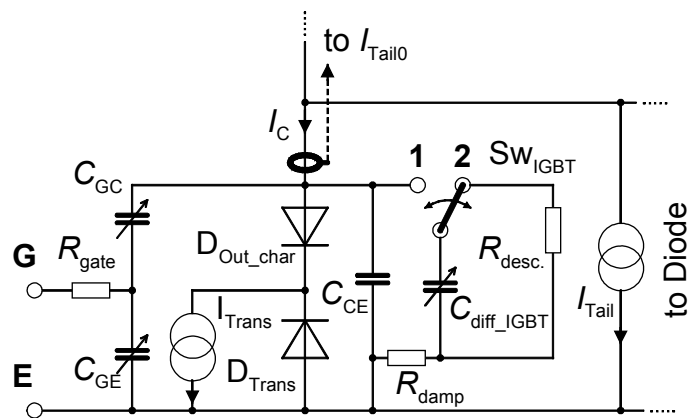


Figure 3.8: Test setup for IGBT switching characteristics



(a)



(b)

Figure 3.9: Measured vs. simulated  $V_{CE}$  for turn-off transient without (a) and with (b)  $C_{diff\_IGBT}$



observed. Rise and fall times are calculated between 10% and 90% of the steady-state value. The simulated and measured current slopes are compared directly while the collector-emitter electrical charge is calculated from the  $I_C$  integral.

### 3.2.1.1 IGBT Turn-off transient

The measured and simulated  $V_{CE}$  curves are illustrated in Figure 3.9 (a). It can be noticed that the error is large: the measured  $t_{r\_mes} = 121$  ns and simulated  $t_{r\_sim} = 37$  ns rise times. The simplified simulation model fails in this case mainly because the diffusion capacity of the drift region, determined by the **pn** junction  $J_1$  from Figure 2.1 (a), was neglected in the first instance. Before  $V_{CE}$  reaches the DC-link level, this region is swamped with carriers as the current is forced to flow through the IGBT (the freewheel diode does not conduct). Thus, the  $V_{CE}$  slope is influenced by the diffusion capacitance (which is a charge-dependent capacitance) during the voltage rise.

To include this effect in the simulation model, an additional capacitance,  $C_{diff\_IGBT}$ , is connected in parallel to  $C_{CE}$ , see Figure 3.9 (b). The effect of this capacitance has to be selected only for the IGBT turn-off transient. Therefore, the switch  $Sw_{IGBT}$  is used. When IGBT is conducting,  $Sw_{IGBT}$  is connecting  $C_{diff\_IGBT}$  to  $R_{desc.}$ , maintaining the capacitance discharged (position 2). At the beginning of the turn-off transient, the switch is commuted to position 1 and  $C_{diff\_IGBT}$  is charging in parallel with  $C_{CE}$ . This will delay the rise of  $V_{CE}$ . After the transition is finished and  $V_{CE}$  remains constant, the switch is commuted again to the initial position in order to discharge  $C_{diff\_IGBT}$  on  $R_{desc.}$ . Thus, the capacitance  $C_{diff\_IGBT}$  is prepared for the next turn-off transient. A very small resistance  $R_{damp}$  (1 m $\Omega$ ) is used to prevent numerical errors during the simulation.

Following principle was used to parameterize  $C_{diff\_IGBT}$ : the diffusion capacitances are depending on the stored charged in the drift region [25], [57]:

$$C_{diff\_IGBT} = \frac{dQ}{dV_{CE}} \approx \tau_{Cr} \cdot \frac{I_C}{V_T} = f(I_C), \quad \text{Eq. 3.1}$$

where  $\tau_{Cr}$  is the carrier lifetime and  $V_T$  represents the thermal voltage of the collector side **pn** junction. In other words,  $C_{diff\_IGBT}$  takes different values for different current levels. Measurements were used here to calculate the capacitance value from charge difference  $\Delta Q$  (integral of  $I_C$ ) and voltage difference  $\Delta V_{CE}$  between time instants  $t_1$  and  $t_2$ , see Figure 3.9 (a), assuming a constant  $I_C$  during  $dV_{CE}/dt$ . Between these points,  $V_{CE}$  transient is

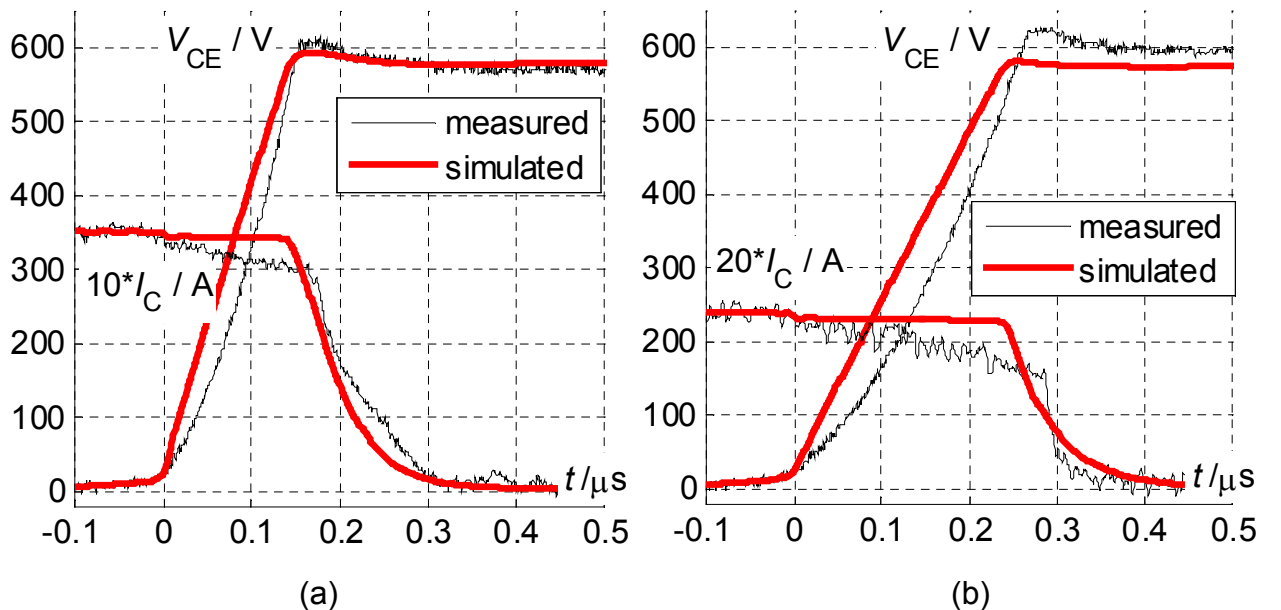


Figure 3.10: Measured vs. simulated  $V_{CE}$  during turn off for  $I_C = 35A$  (a) and  $I_C = 12A$  (b)

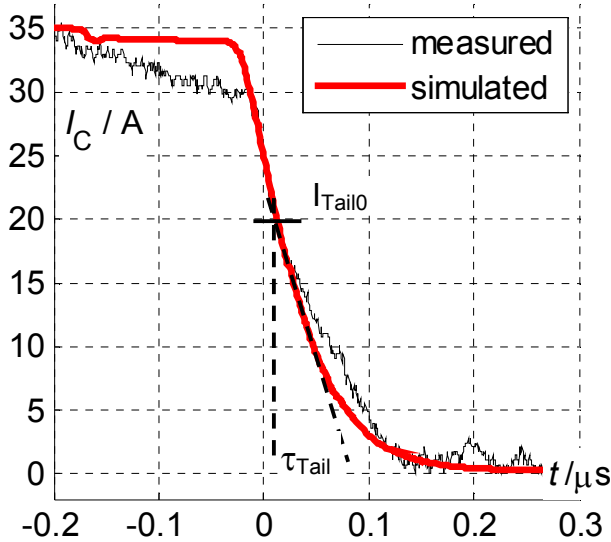


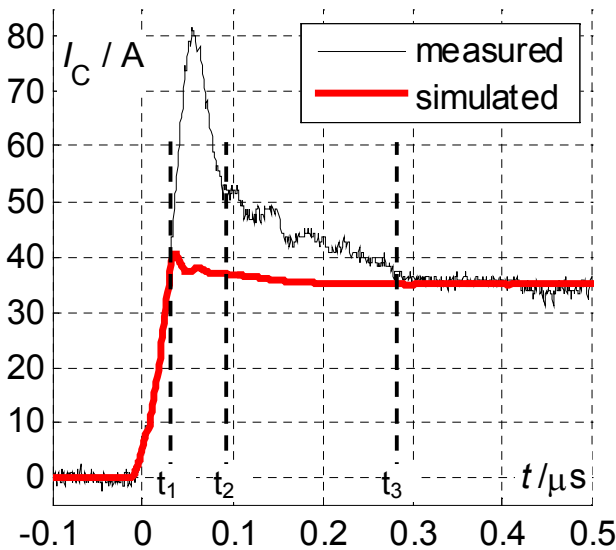
Figure 3.11: Collector current at turn-off (35A)

mostly influenced by the diffusion capacitance. The results for the selected current levels are then interpolated using a look-up table with current as input and capacitance as output. Thus, a capacitance-current dependency is obtained for the chosen hard-switching condition (see Table 3.2): optimal gate resistance  $R_G = 22 \Omega$  given in the data sheet and current levels below maximal value (70 A for the selected IGBT module). The simulations and measurements are compared in Figure 3.10 for different current levels. The obtained measured and simulated rise times for  $V_{CE}$  are listed in Table 3.2.

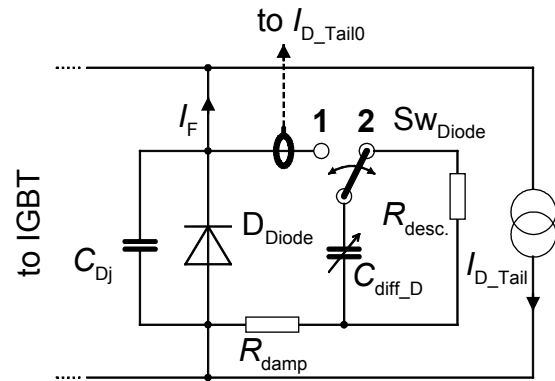
From Figure 3.10 it can be noticed that  $dV_{CE}/dt$  varies with the current level, roughly with the root of  $I_C$  [24]. Despite the fact that, the capacitance  $C_{diff\_IGBT}$  is smaller for lower  $I_C$  levels (see Table 3.2), the voltage slope is smaller also because the lower collector current is used to charge this capacitance during the turn-off transient. Moreover, due to the constant capacitance value, adopted during the turn-off transient, the simulated voltage slope is constant. On the contrary, the measured slope is slightly increasing indicating a change in the diffusion capacitance value. More accurate result may be obtained if the physical equations are implied, but this leads further to complexity increase

Table 3.2: Determined diffusion capacitance dependent on  $I_C$  current level; measured vs. simulated rise times for  $V_{CE}$

$I_C / A$	50.5	35	22.3	12
$C_{diff\_IGBT} / nF$	9.9	9	7	4.9
$t_{r\_mes} / ns$	95.2	121	150	207
$t_{r\_sim} / ns$	91	117	145	199



(a)



(b)

Figure 3.12: Measured vs. simulated  $I_C$  for turn-on transient without (a) and with (b)  $C_{diff\_D}$

of the simulation model, which is beyond the purpose of this work. As already explained, the physics-based IGBT models are difficult to parameterize.

Another aspect, regarding the turn-off transient, represents the parameterization of the tail-current circuit. From the measurement of the collector current, at 35 A level, the constant time  $\tau_{\text{Tail}}$  and the initial value  $I_{\text{Tail0}}$  are determined [25], [27]. Shown in Figure 3.11, these parameters are found to be:  $\tau_{\text{Tail}} \approx 70 \text{ ns}$  and  $I_{\text{Tail0}} \approx 0.55 \cdot I_C$ . The current waveforms from Figure 3.10 show a good agreement between measurements and simulations for different current levels with the parameterized tail-current network.

### 3.2.1.2 IGBT Turn-on transient

Using the simplified model from Figure 2.9 (a), the results for the collector-current transient during turn-on are presented in Figure 3.12 (a). A large difference between measurements and simulations can be noticed regarding the reverse-recovery effect of the freewheel diode [57]. While the lower IGBT starts to conduct, the upper diode goes into blocking state. The diode current drops towards zero. The drift region of diode's *pn* junction is swamped with carriers, which cannot vanish immediately. Therefore the diode

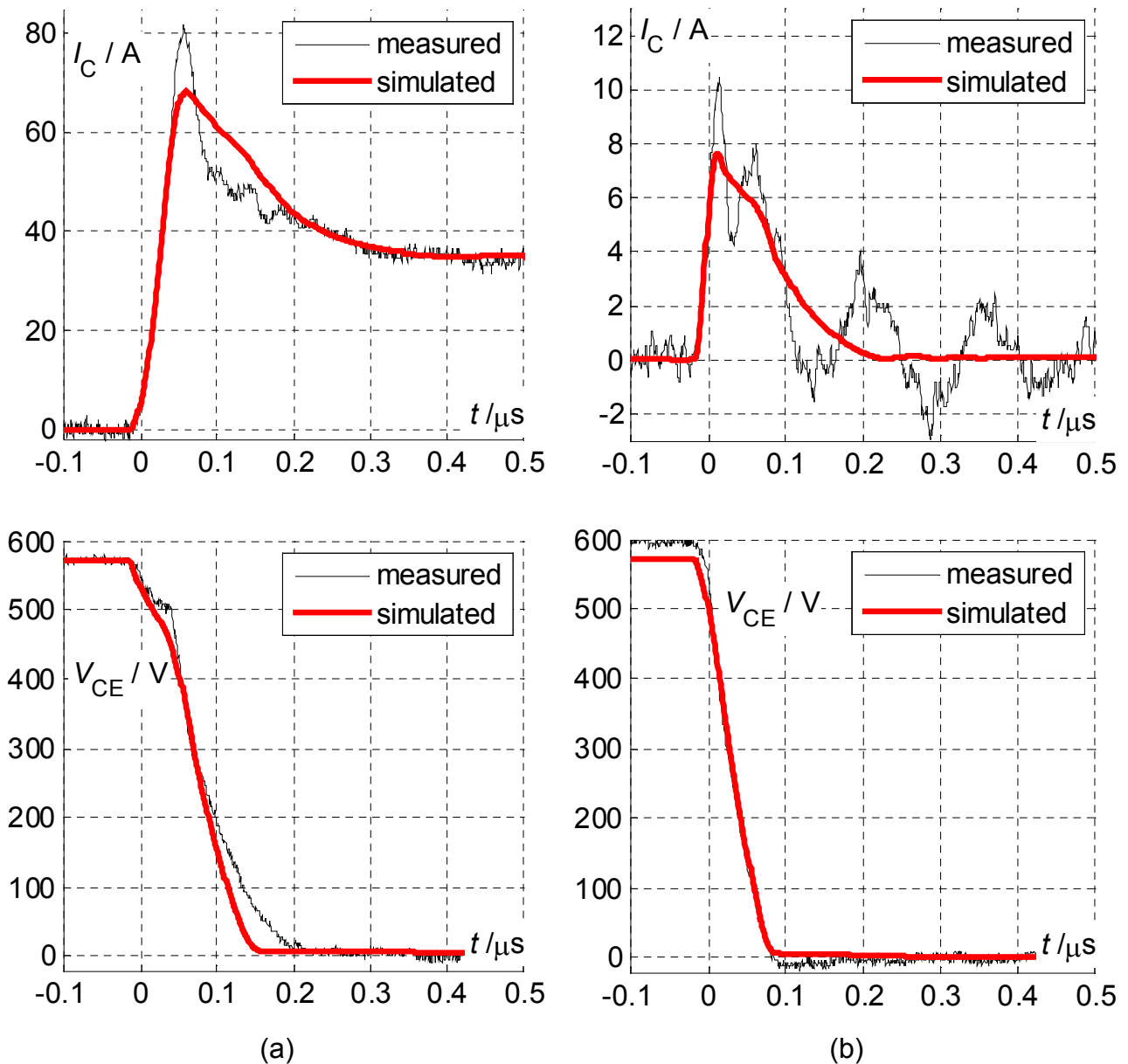


Figure 3.13: Measured vs. simulated  $V_{CE}$  and  $I_C$  during turn on for  $I_C = 35\text{A}$  (a) and  $I_C = 0\text{A}$  (b)

**Table 3.3: Determined diode's diffusion capacitance dependent on  $I_F$  current level; measured vs. simulated reverse-recovery el. charge; measured vs. simulated fall times for  $V_{CE}$** 

$I_F / A$	35	21.5	10.8	0
$C_{diff\_D} / nF$	3.4	2.8	2.3	0.54
$Q_{rr\_mes} / \mu C$	3.7	3.3	2.52	0.72
$Q_{rr\_sim} / \mu C$	4.2	3.42	2.85	0.74
$t_f\_mes / ns$	141	102	83	63
$t_f\_sim / ns$	118	90	85	69

current will start to flow in the negative direction until all carriers are swept out. This effect is also known as reverse recovery. Responsible for it is the diffusion capacitance of the diode, which was neglected previously in the simulation model. This capacitance is reflecting the amount of electric charge stored before the turn-off transient.

To model the reverse-recovery effect, an approach, similar to the IGBT case, is adopted, see Figure 3.12 (b): the capacitance  $C_{diff\_D}$  is connected in parallel to the junction capacitance  $C_{Dj}$  of the diode. The switch  $Sw_{Diode}$  is used to connect this capacitance only when the diode turn-off transient starts (to isolate the effect of  $C_{diff\_D}$  from IGBT turn-off transient). The principle is similar like in  $C_{diff\_IGBT}$  case: when diode is conducting,  $Sw_{Diode}$  is in position **2** maintaining  $C_{diff\_D}$  discharged. If the diode forward current  $I_F$  becomes negative,  $Sw_{Diode}$  commutates to position **1** and  $C_{diff\_D}$  charges in parallel with  $C_{Dj}$ , allowing a negative current flow with respect to  $I_F$  direction.

Additionally, a similar tail-current network is used to maintain a slow current decay to the steady-state value, like in IGBT turn-off case. After the IGBT turn-on transient is over (turn-off transient of the freewheel diode),  $Sw_{Diode}$  commutates back to position **2** discharging  $C_{diff\_D}$  and waiting for next turn-off transient. Also here, a small resistance  $R_{damp}$  is used to avoid numerical errors during the simulation. The parameterization of  $C_{diff\_D}$  is done in a same way as for  $C_{diff\_IGBT}$ , based on Eq. 3.1. The electric charge difference  $\Delta Q_{el}$  is calculated between the time intervals  $t_1$  and  $t_2$ , shown in Figure 3.12 (a), and, dividing it to the voltage difference (app. DC-link level), the capacitance value for  $C_{diff\_D}$  is obtained. The tail-current network is also parameterized. Between  $t_2$  and  $t_3$ , the time constant  $\tau_{Tail\_D} \approx 60ns$  and initial current  $I_{Tail0\_D} \approx 0,5 \cdot I_{RRM}$  are obtained.

In Figure 3.13, the simulated and measured current and voltage waveforms are compared for different steady-state collector-current values. The values for the simulated and measured reverse-recovery electric charge ( $Q_{rr\_sim}$  and  $Q_{rr\_mes}$ ) and the fall time ( $t_f\_sim$  and  $t_f\_mes$ ) of the voltage  $V_{CE}$  (between 10% and 90% from steady-state value) are summarized in Table 3.3 for the corresponding IGBT. Here, a direct relation between reverse-recovery energy ( $C_{diff\_D}$  value) and voltage fall times is observed.

Similar drawback, like in the case of IGBT, is noticed: due to the constant value for  $C_{diff\_D}$ , adopted during the diode turn-off transient, the peak of the reverse-recovery current is not simulated. Instead the total reverse-recovery energy (electric charge) needs to be simulated to obtain a good approximation of the IGBT turn-on losses.

Concluding, the IGBT behavioral model was extended with an auxiliary network to include the effects of the diffusion capacitance, as this influences the voltage gradient during the turn-off transient, depending on the steady-state level of the collector current before transition. Similar phenomena lead to a second problem: simulation of reverse-recovery effect during the diode turn-off transient. By adding an additional network to the diode model, a parallel capacitance delivers the necessary electric charge during this transient. Ideal switches are used in this case to avoid the interaction between turn-off transients of IGBT and diode. The capacitance values are obtained from measurements at the real module. However, it must be considered that these measurements were conducted only for the optimal gate resistance value. This optimal resistance value is found in datasheet and will be further used.

### 3.2.2 Cable simulations and measurements

To check the cable simulation model, comparisons with measurements are necessary. The test setup configuration (buck converter topology with inductive load) from the previous section is driven with a short train of pulses, but having the load connected via two conductors from the long cable, see Figure 3.14. Thus, tests are possible for different collector current levels.

Important aspects in modeling the cable, like the parameter variation with frequency, the number of  $\Gamma$  sections and the length and topology of the cable, are discussed further in detail. Model improvements are also presented by comparing the measured and simulated voltage at the inverter output/load (motor) input and the collector current.

#### 3.2.2.1 Parameters variation with frequency

The most known effect, when increasing the frequency, represents the skin effect. At high frequencies, the current tends to flow at the surface of the conductor. This causes an increase of the conductor resistance (current flows only through a part of conductor cross section) and reduction of the conductor inductance due to the decrease of the internal inductance. Another phenomenon, met in bundle connections of conductors, is the proximity effect. This effect influences the current flow in two adjacent conductors in such way that, for high frequencies, the currents tend to flow only on the side facing the neighbor conductor. Thus, the resistance is increased further. Also, in the case of two adjacent conductors with currents in opposite direction, the mutual inductance between those two conductors reduces further the loop inductance.

Another phenomenon is observed for the cable capacitances: the capacitance value decreases with increasing frequency, explained by the polarization process of the dielectric, which depends on the frequency [58]. Because the polarization sequence of the dielectric molecules needs a certain time, the dipoles cannot follow the alternating electric field, which excites them, at high frequency and finally the electrical permittivity decreases. Although in many references this phenomenon is neglected [52] [33], because the capacitance variation is small (app 10%) and electrical conductivity remains negligible (less than 1mS/m), this may lead to inaccurate estimation of the traveling wave velocity.

To exemplify these phenomena, the frequency dependence of the parameters is analyzed for a 5-conductor shielded cable (34m-long LAPP). The influence of both skin and proximity effects can be seen in Figure 3.15, where the measured loop resistance  $R_A$  and inductance  $L_A$  (see Eq. 2.45) are plotted together with the calculated ones (using the method from [52]). This analytical method was presented in section 2.2.5. It can be noticed that the calculated inductance is larger than the measured one for the entire frequency spectrum considered (Figure 3.15 (a)). Further, the calculated resistance is much larger at low frequencies (1 kHz) than the measured one ( $R_{A\_calc.} \approx 55 \text{ m}\Omega/\text{m}$ ,  $R_{A\_mes.} \approx 17 \text{ m}\Omega/\text{m}$ ),

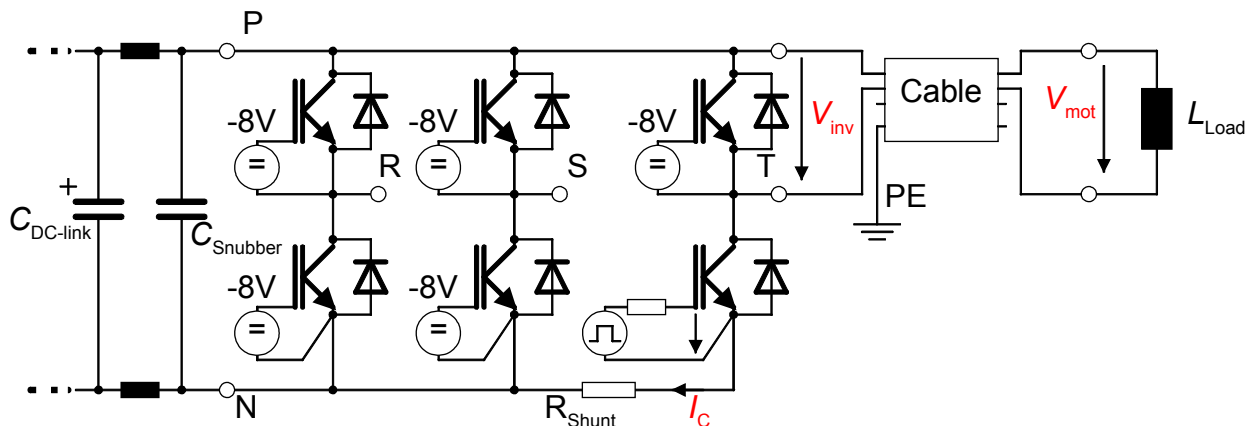


Figure 3.14: Test setup for measurements of the voltage and current wave propagation.

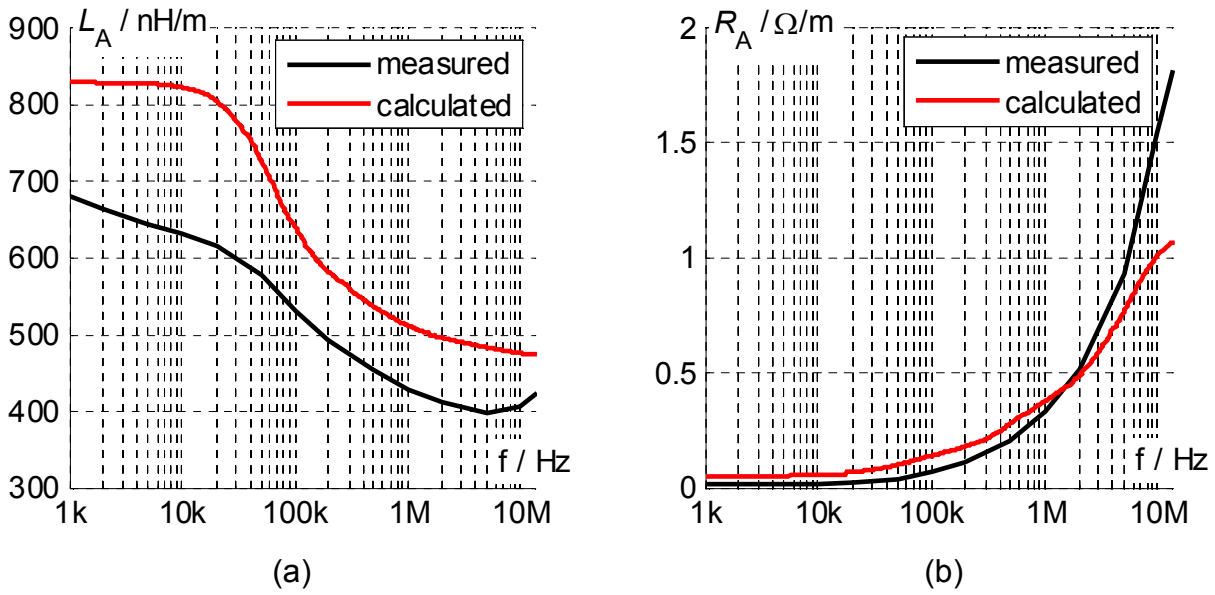


Figure 3.15: Measured and simulated inductance (a) and resistance (b) of the cable.

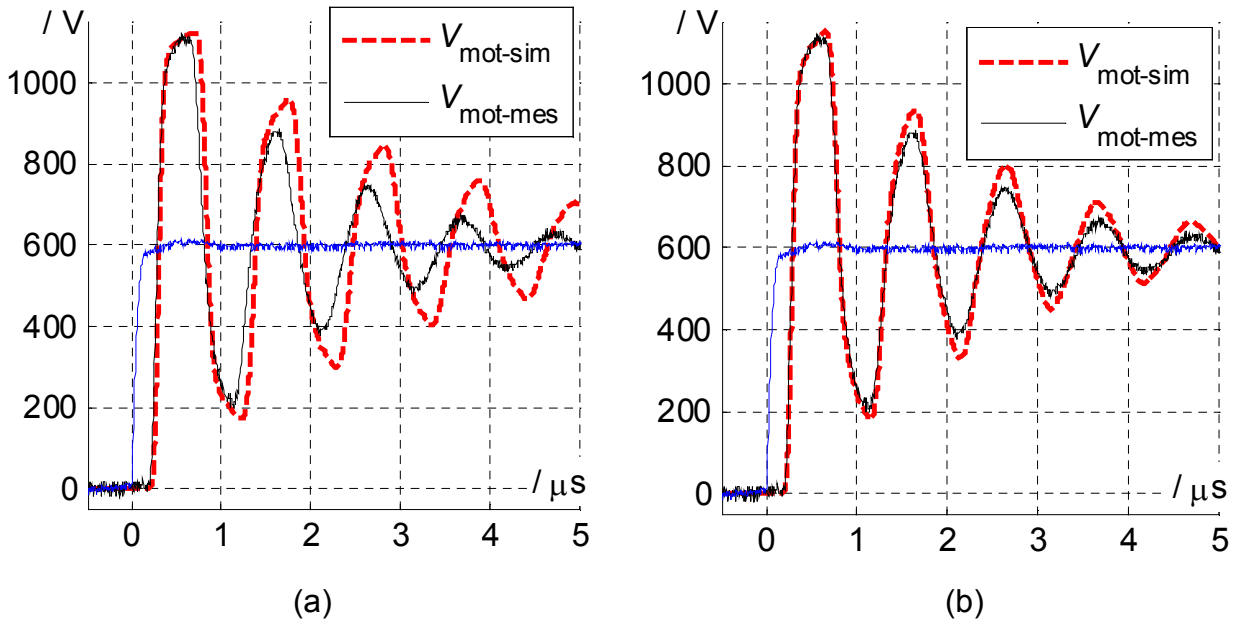
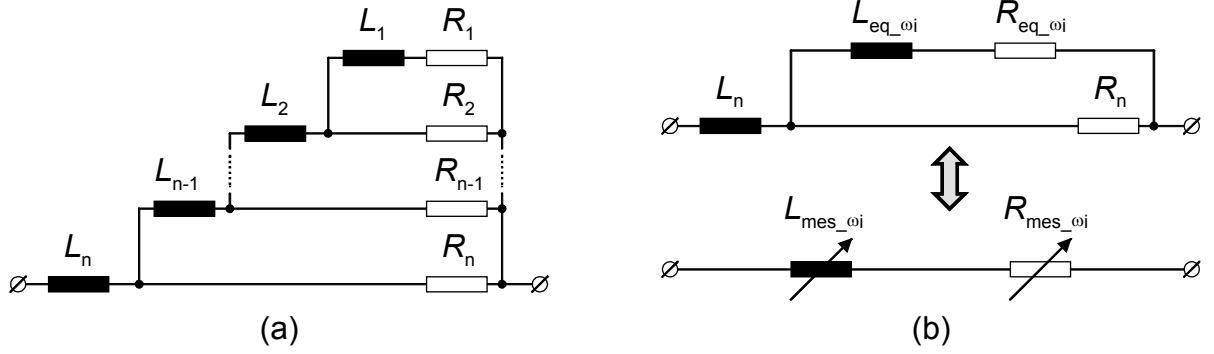


Figure 3.16: Measured and simulated voltage reflections at motor with model from: (a) [52]; (b) [33]

which causes large steady-state voltage drops across the cable for high current values (Figure 3.15 (b)). On the contrary, at high frequencies (10 MHz), the calculated AC resistance is lower than the measured one ( $R_{A\_calc.} \approx 1.01 \Omega/m$ ,  $R_{A\_mes.} \approx 1.537 \Omega/m$ ) and thus, the simulated attenuation of the voltage reflections at the motor input is less than the measured one, see Figure 3.16 (a). Also here, the mismatch between measured and simulated cable inductance leads to a mismatch of the cable natural frequency, i.e. a higher calculated inductance  $L_{calc.}$  leads to a lower oscillation frequency, see Eq. 2.23.

A different approach to calculate the cable parameters was presented in [33], where a similar representation of the conductor's cross-section is adopted using a RL ladder circuit to simulate the resistance and inductance variation with frequency. In this case the parameterization of the RL ladder circuit starts from the values of the measured resistance and inductance, continuing with an iterative process, also called sequential order reduction of the system of equations. Thus, a curve fitting of the measured parameter values is realized. The advantage is that the calculated values, using finite element methods, can replace the measured values, leading to good results.



**Figure 3.17: RL ladder circuit with  $n$  branches (a) and equivalent reduction of  $n-1$  branches (b)**

The ladder circuit is presented in Figure 3.17 (a) for a number of  $n$  branches. The measured values,  $R_{mes\_oi}$  and  $L_{mes\_oi}$ , are given for  $n$  frequencies ( $i = 1 \dots n$ ), defining the frequency range ( $n^{th}$  – highest and  $1^{st}$  – lowest) for the desired variation of parameters. Thus, the number of data pairs for each frequency is equal to the number of branches. In Figure 3.17 (b), the  $n-1$  branches are grouped in a single branch with an equivalent resistance  $R_{eq\_oi}$  and inductance  $L_{eq\_oi}$ , also for the entire frequency range. The algorithm, detailed in [33], is based on the following steps:

a) the parameters for the  $n^{th}$  branch are calculated from the measured parameters at the  $n^{th}$  and  $(n-1)^{th}$  frequency, using the following relations:

$$\Delta L = L_{mes\_oi} - L_{mes\_oi-1},$$

$$\Delta R = R_{mes\_oi} - R_{mes\_oi-1},$$

$$L_n = L_{mes\_oi-1} - \frac{\Delta L \cdot [(\Delta R / \Delta L)^2 + \omega_n^2]}{(\omega_n^2 - \omega_{n-1}^2)}, \quad \text{Eq. 3.2}$$

$$R_n = \frac{\Delta R}{\Delta L} \cdot (L_{mes\_oi} - L_n) + R_{mes\_oi}, \quad \text{Eq. 3.3}$$

where  $\omega_n = 2\pi \cdot f_n$  represents the highest frequency;  $\Delta L$  and  $\Delta R$  are the differences of the measured inductance and resistance at the frequency  $n$  and  $n-1$ .

b) the equivalent resistance and inductance of the rest  $n-1$  branches are calculated for all  $n-1$  remained frequencies:

$$L_{eq\_oi} = \frac{R_n \cdot (L_{mes\_oi} - L_n)}{(R_n - R_{mes\_oi})^2 + \omega_i^2 \cdot (L_{mes\_oi} - L_n)^2}, \quad \text{Eq. 3.4}$$

$$R_{eq\_oi} = \frac{R_n \cdot [R_n \cdot R_{mes\_oi} - R_{mes\_oi}^2 - \omega_i^2 \cdot (L_{mes\_oi} - L_n)^2]}{(R_n - R_{mes\_oi})^2 + \omega_i^2 \cdot (L_{mes\_oi} - L_n)^2}, \quad \text{Eq. 3.5}$$

where  $i = 1 \dots n-1$ .

c)  $L_{eq\_oi}$  and  $R_{eq\_oi}$  are used further to obtain the parameters for the  $(n-1)^{th}$  branch, replacing  $L_{mes\_oi}$  and  $R_{mes\_oi}$  in Eq. 3.2 and Eq. 3.3 ( $i = 1 \dots n-1$ ).

The steps b) and c) are repeated until the order of the system is reduced to 2. One can interpret this successive repetition of the steps b) and c) as an extraction of each concentric circle, starting with the exterior one, until the inner 2 concentric sections remain.

d) having only two branches left, the parameters for first and second branch are calculated using the following equations:

$$\Delta L' = L'_{eq\_oi} - L'_{eq\_oi-1},$$

$$\Delta R' = R'_{eq\_oi} - R'_{eq\_oi-1},$$

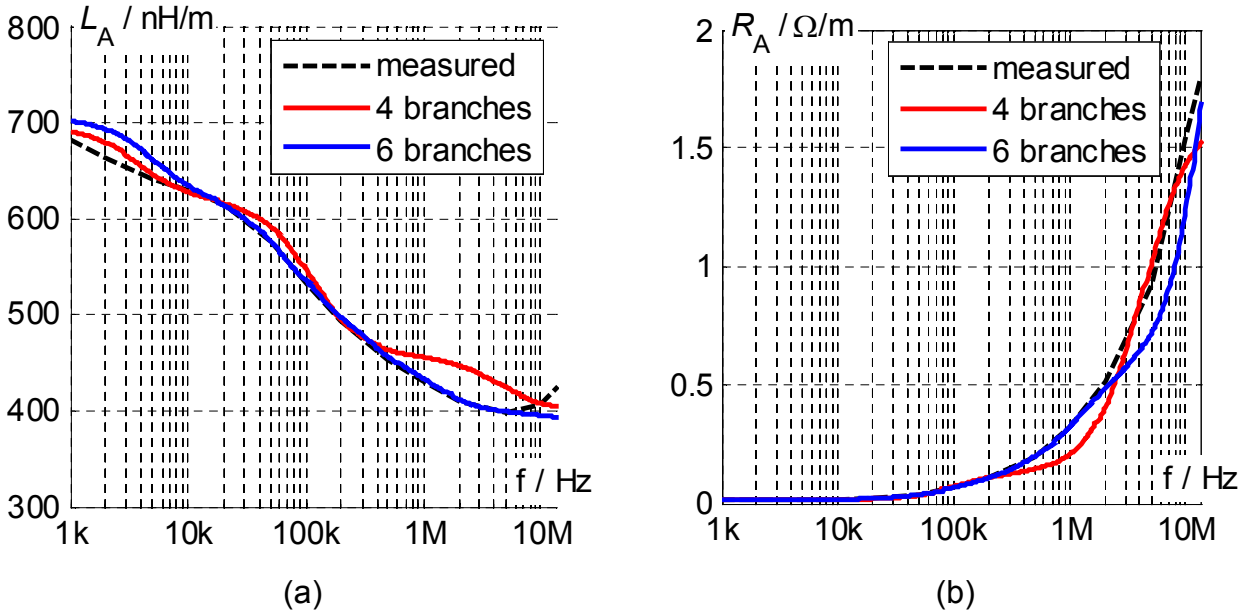


Figure 3.18: Measured and calculated impedance  $L_A$  (a) and resistance  $R_A$  (b)

$$L_2 = L'_{eq\_w_1} - \frac{\Delta L' \cdot [(\Delta R' / \Delta L')^2 + \omega_2^2]}{(\omega_2^2 - \omega_1^2)}, \quad \text{Eq. 3.6}$$

$$R_2 = \frac{\Delta R'}{\Delta L'} \cdot (L'_{eq\_w_2} - L_2) + R'_{eq\_w_2}, \quad \text{Eq. 3.7}$$

$$L_1 = \frac{R_2^2 \cdot (\omega_2^2 - \omega_1^2)}{\Delta L' \cdot [(\Delta R' / \Delta L')^2 + \omega_1^2] \cdot [(\Delta R' / \Delta L')^2 + \omega_2^2]}, \quad \text{Eq. 3.8}$$

$$R_1 = L_1 \cdot \frac{\Delta R'}{\Delta L'} - R_2. \quad \text{Eq. 3.9}$$

Here,  $L'_{eq\_w_1}$ ,  $L'_{eq\_w_2}$ ,  $R'_{eq\_w_1}$  and  $R'_{eq\_w_2}$  are the equivalent parameters of the remaining branches 1 and 2 connected together for the lowest frequencies  $\omega_1$  and  $\omega_2$ , respectively ( $\omega_1 < \omega_2 < \dots < \omega_n$ ).

Finally, the choice of the branches number represents an iterative optimization process. The authors recommend in [33] to choose the frequencies in a proportional progress, i.e.  $\omega_n / \omega_{n-1} = \omega_{n-1} / \omega_{n-2} = \dots = \omega_2 / \omega_1$ . Moreover, with increased number of branches, higher accuracy is obtained but also negative parameter values. Despite their physical meaningless, the negative parameter values combined together with the positive values deliver good results for total network inductance and resistance. In Figure 3.18, the

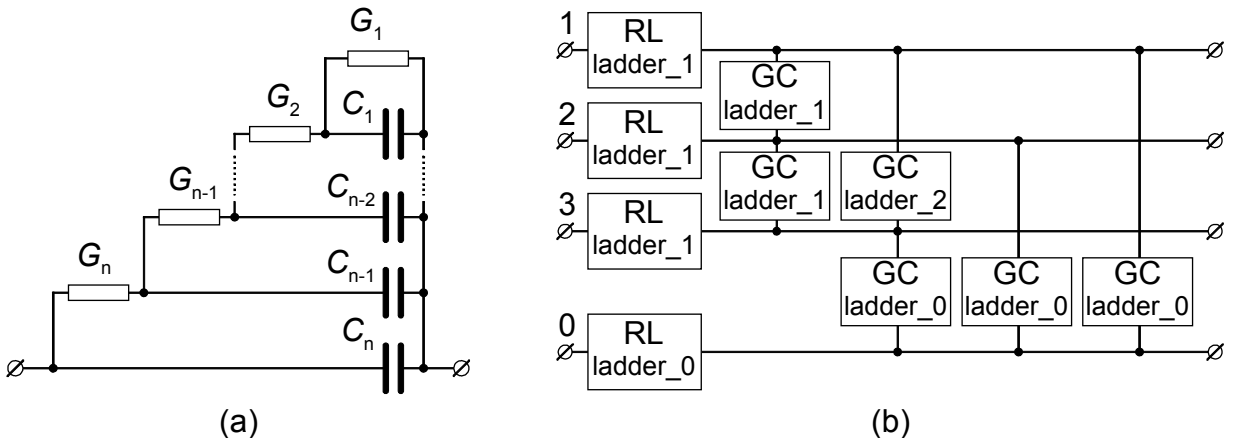


Figure 3.19: GC ladder circuit (a) and complete cable model with RL and CG ladder circuits (b)



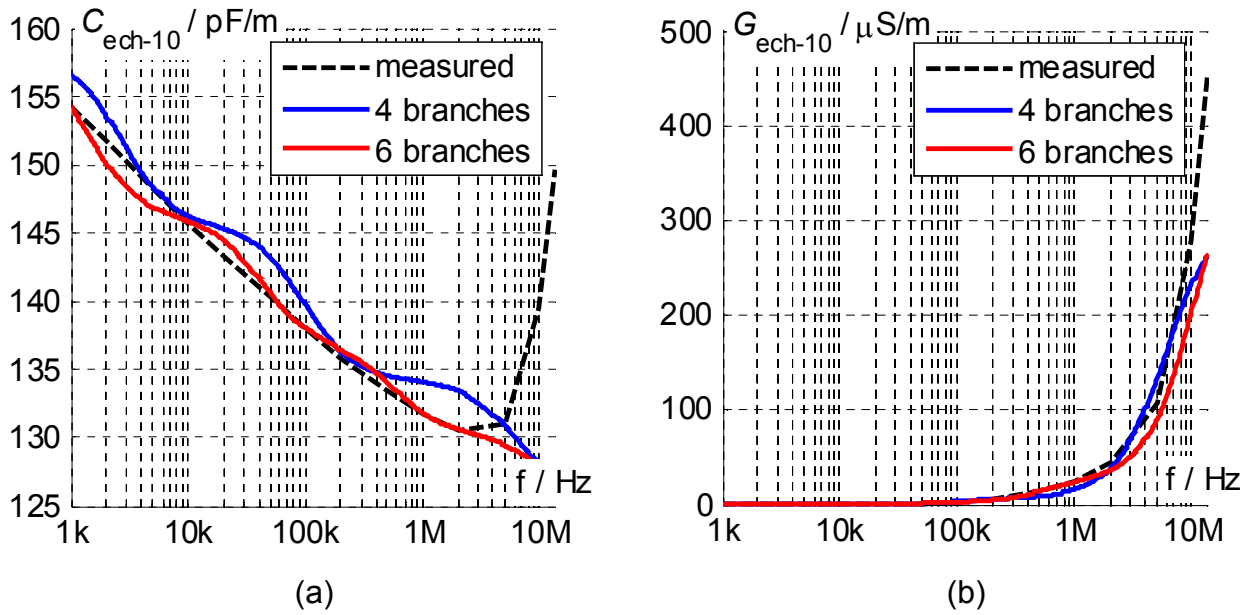


Figure 3.20: Measured and calculated capacitance  $C_{ech-10}$  (a) and conductance  $G_{ech-10}$  (b)

measured and calculated inductance/resistance are plotted for  $L_A$  and  $R_A$ , respectively.

[53] shows that the same method can be adapted and applied for capacitances and conductances. Previously, the cable capacitances have been considered constant and conductances have been neglected due to their small value, see Figure 2.22 (b). From measurements it can be noticed that the capacitance value decreases with frequency. The conductance, however, increases with almost four orders of magnitude. The equations from the previous case, Eq. 3.2 to Eq. 3.9, are valid also here by replacing  $R$  with  $G$  and  $L$  with  $C$  in a parallel connection, under the consideration of the ladder circuit from Figure 3.19 (a). In this case the equations are derived from the equivalent admittance of the ladder circuit. In Figure 3.19 (b), the complete cable simulation model is illustrated, made up of RL and GC ladder circuits. The parameters depend on the cable configuration, e.g. *GC\_ladder\_1* stands for the capacitance between neighboring conductors and *GC\_ladder\_2* for the capacitance between distant conductors. Additionally, the equivalent inductance of the shield and remaining conductors connected to the ground is considered, using *RL\_ladder\_0*. This influences the CM voltage and ground current waveform.

In Figure 3.20 the frequency dependence of the conductor-ground equivalent capacitance  $C_{ech-1-0}$  and conductance  $G_{ech-1-0}$  is given for the *LAPP Classic 115CY* cable. In Appendix, section 7.1.1, is shown how to obtain the individual capacitances  $C_0$ ,  $C_1$  and  $C_2$  from the measured  $C_A$ ,  $C_B$  and  $C_C$ . Also there, the expressions for the conductor-ground equivalent capacitances  $C_{ech-i-0}$  ( $i = 1 \dots 3$ ) are shown for the general case of shielded cables with five conductors. It can be noticed that the 6-branch model delivers more accurate results than 4-branch. The measured capacitance indicates an imminent resonance point after 10 MHz, which has to be avoided due to wrong capacitance values.

After connecting the simulation model of the cable from Figure 3.19 (b) (6-branch ladder circuits) to inverter and load inductance model, the results from Figure 3.16 (b) are obtained. It can be noticed that the AC resistance is much better approximated. Moreover, the oscillation period of the voltage wave is simulated accurately, indicating a good match of the inductances and capacitances of the cable.

### 3.2.2.2 Effect of the IGBT collector current on collector-emitter voltage slope

As already presented in subsection 3.2.1.1, the collector current influences the voltage slope of the collector-emitter voltage during the turn-off transient. Thus, the small steady-state values, before the turn-off transient, cause smaller voltage gradients than the large ones, see Figure 3.10. When the cable is connected at the inverter output, it affects the

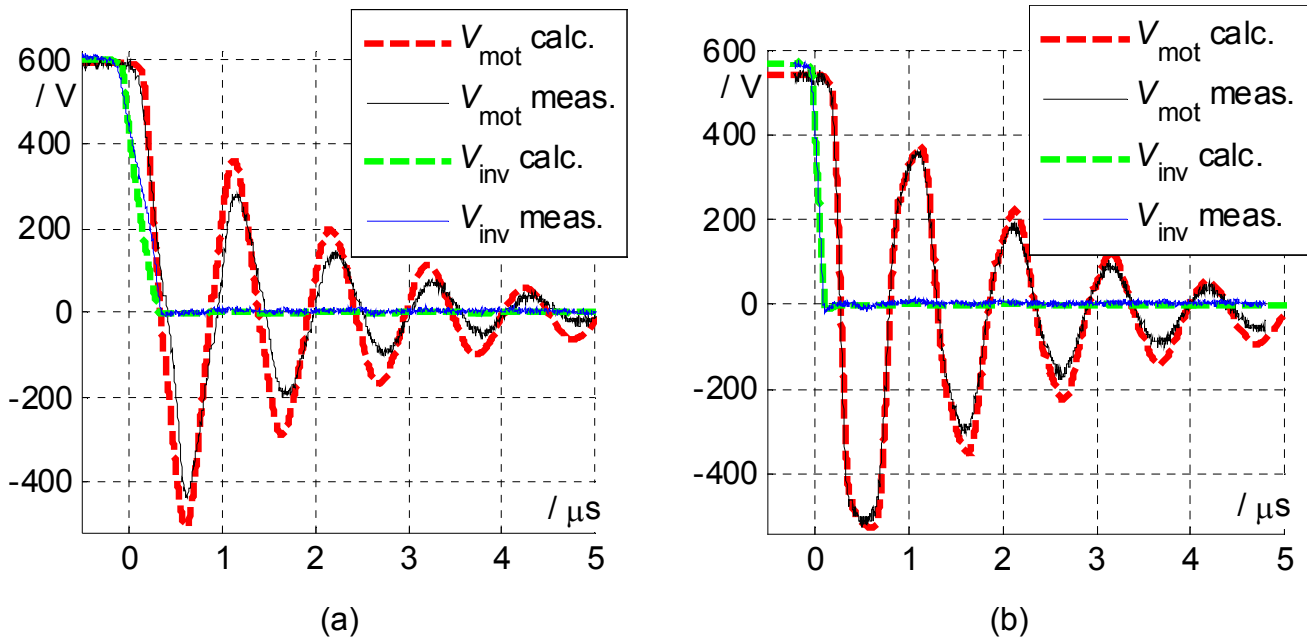


Figure 3.21: Voltage reflections at motor input for turn-off transient at 13A (a) and 50A (b)

traveling voltage waveforms, especially those shorter than 50 m. A comparison is shown in Figure 3.21 between the IGBT turn-off transients at  $I_C \approx 13$  A and  $I_C \approx 50$  A. A voltage gradient is observed ( $\approx 1.2$  kV/ $\mu$ s) for smaller current, leading to a fall time  $t_r \approx 408$  ns. When comparing with the wave propagation time  $t_p \approx 220$  ns, from section 7.1.1 in Table 7.3 (Appendix), Eq. 2.29 becomes valid. It can be noticed that the peak of the voltage reflection is derated, not only by the reflection coefficient  $K_L$  but also by the  $t_r / t_p$  factor. With increased current level (50 A), the voltage gradient increases to app. 4.175 kV/ $\mu$ s. Here, the Eq. 2.30 is valid and the peak of the voltage reflection depends only on  $K_L$ . It must be kept in mind that  $V_{inv}$  represents the reverse-bias voltage of freewheeling diode; see Figure 3.14. When compared, the obtained voltage gradients during the IGBT turn-off transitions are smaller or equal to the ones from the turn-on transitions, see Figure 3.16.

Finally it can be concluded, that the biggest voltage slope occurs during the turn-on transient of the hard-switched IGBT. Thus, considering the condition for the total reflection of the voltage from Eq. 2.30, the turn-on IGBT transients are found to be the worst case for the double effect of the voltage, starting already for short cables, e.g. in this case less than 34 m. Therefore, only the IGBT turn-on transients will be considered further in chapter 4, where several measures for overvoltage reduction are studied.

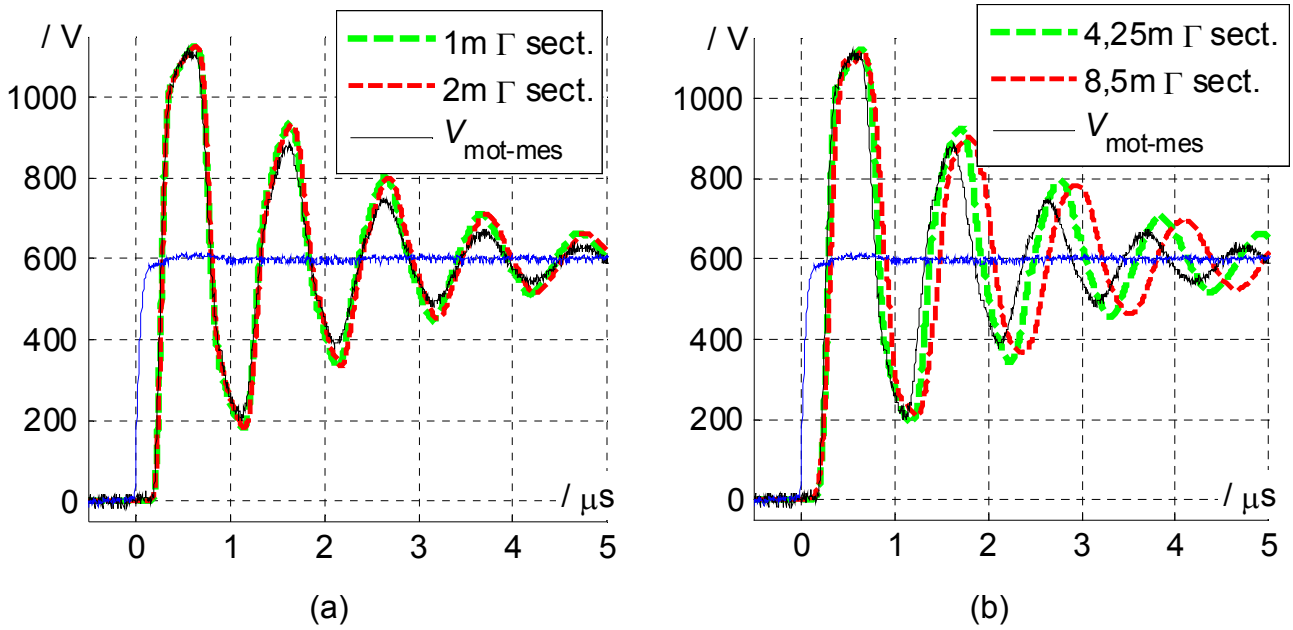
### 3.2.2.3 Effect of the length of the cable $\Gamma$ sections

The expressions for the optimal number of  $\Gamma$  sections were presented in section 2.2.2. There, a critical value  $l_{crit}$  of the section length was found to be directly related to the cable parameters, see Eq. 2.28. For exemplification, the LAPP Classic 115CY cable (34 m) is considered. The propagation speed of the voltage waveform is given in Appendix, (in Table 7.3):  $v_{C\_calc\_min} \approx 139$  m/ $\mu$ s. The voltage transient time (rise or fall) is found to be most critical during the turn-on transition. Without the cable connected at the inverter output, the fastest transition is found in Table 3.3 from subsection 3.2.1.2:  $t_{f\_min} \approx 70$  ns. Now the minimum wavelength can be calculated using Eq. 2.26:  $\lambda_{min} \approx 10$  m.

Inserting the calculated  $\lambda_{min}$  in Eq. 2.27, the critical length for LAPP cable is found to be:

$$l_{crit} = X \cdot \lambda_{min} = X \cdot 10 \text{ m} = \begin{cases} 2 \text{ m, for } X = 1/5, \\ 1 \text{ m, for } X = 1/10. \end{cases}$$

The factor  $X$  has been presented previous and should be minimum 1/5. A recommended value of 1/10 is also considerable. Simulation results for different lengths



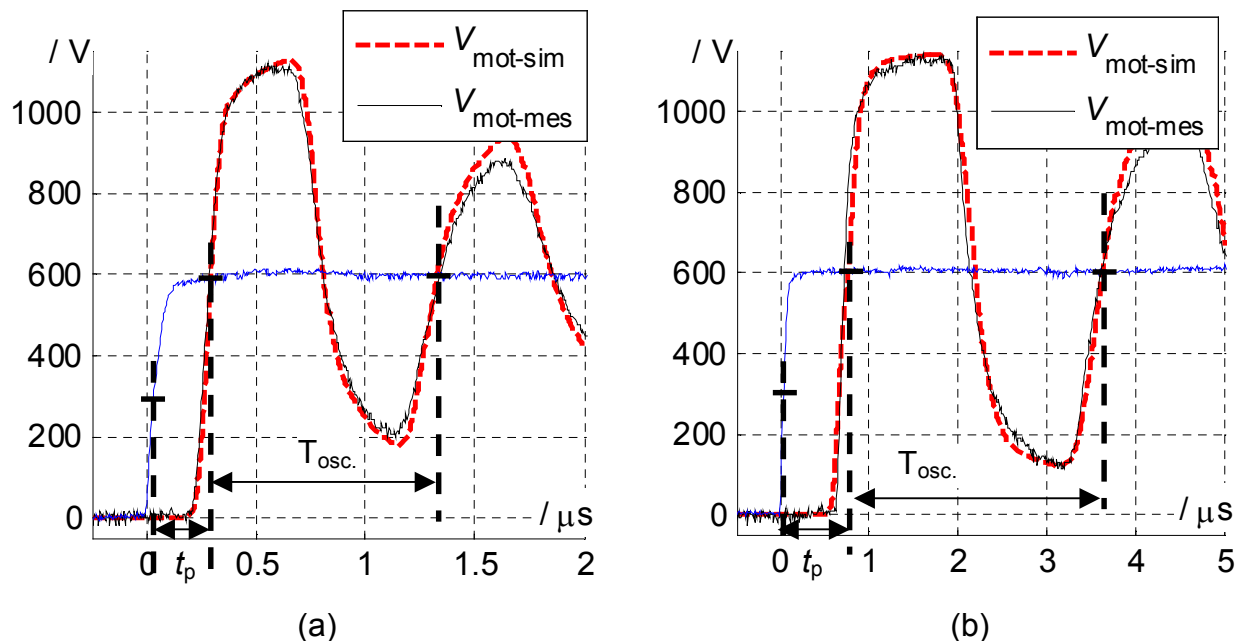
**Figure 3.22: Simulated vs. measured voltage reflections for  $\Gamma$  sections of 1 and 2m (a); 4 and 8.5m (b)**

$I_{crit}$  are shown in Figure 3.22. It can be noticed that for sections of 1 m, the results are optimal. Also the 2 m long section gives satisfactory results, although a slight increase of the oscillation period is observed, see Figure 3.22 (a). On the contrary, the 4 m and 8 m section lengths lead to wrong results, noticeable through an important increase of the oscillation period due to the mismatch of the cable parameters for long  $\Gamma$  sections.

### 3.2.2.4 Effect of the cable length

The cable length has an important role in traveling wave phenomena. First, the length determines the oscillation period along the cable, i.e. the wave propagation delay  $t_p$ . Second, the increased length determines higher stray inductance and capacitance, leading to higher displacement currents, especially for shielded cables, and finally to higher losses.

To analyze the effect of the cable length, two cables are considered: *LAPP Classic 115 CY* of 34 m (5-conductor shielded) and *Ozoflex H07RN-F* of 99 m (4-conductor unshielded). The parameters for both cables are detailed in Appendix, sections 7.1.1 and



**Figure 3.23: Voltage reflections at motor terminals using LAPP (a) and Ozoflex (b) cables**

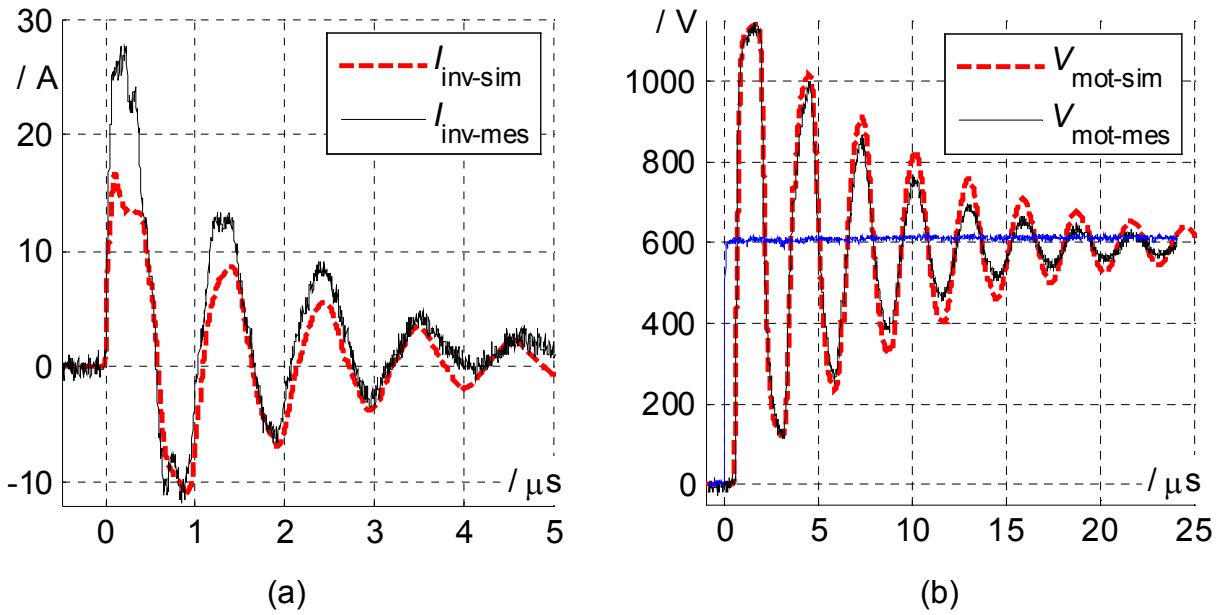


Figure 3.24: Measured vs. simulated current (LAPP cable) (a) and voltage (Ozoflex cable) (b)

7.1.2. The relation between the total length of the cable  $l_{total}$ , the voltage wave propagation speed  $v_c$ , and the propagation delay  $t_p$  has been presented in section 2.2.2, see Eq. 2.24. By inserting the obtained values for parameters we get:

- LAPP cable:  $t_p = l_{total} / v_c \approx 34 \text{ m} / 140 \text{ m} / \mu\text{s} = 243 \text{ ns}$  ;
- Ozoflex cable:  $t_p = l_{total} / v_c \approx 99 \text{ m} / 145 \text{ m} / \mu\text{s} = 683 \text{ ns}$  .

The obtained propagation times can be read easily from the waveform graphics of the measurements vs. simulations characteristic, shown in Figure 3.23. After traveling on the cable 4 times, the wave completes a cycle, corresponding to  $T_{osc} = 4t_p$  for the ideal case ( $K_L \approx 1$ ). Also, the length of the cable can be easily estimated from the previous relations if the propagation speed is calculated using the phase inductance  $L'$  and capacitance  $C'$ .

In Figure 3.24 (a) the measured vs. the simulated displacement current is shown for the LAPP cable. The measurement was conducted between one phase conductor and the ground conductors (4<sup>th</sup>, PE and shield) during the IGBT turn-on transient and without load current. High displacement currents are noticeable due to the high capacitive coupling. Moreover, due to the low output impedance of the inverter, the displacement current reflects at the inverter output in the same way as previously presented in the theoretical considerations from Figure 3.21 (b). Comparing the displacement current waveforms with those of the output voltage, an approximately 90° phase shifting is observed, indicating the dominant capacitive coupling to ground.

Additional, in Figure 3.24 (b), the voltage reflections at the motor end of the cable, using the Ozoflex cable (99 m), are illustrated. A smaller ratio AC resistance /  $L'$  and  $C'$ , compared to the LAPP cable (34 m), can be noticed, considering the longer attenuation time of the reflection peaks. This is explained by the larger conductor diameter (4 mm<sup>2</sup>).

### 3.2.3 Motor simulations and measurements

To test the motor model, several measurements are conducted, first using the same configuration from Figure 3.14, but with the cable connected to two phases of the motor instead of load inductance. In the same time, the motor case is connected, using the cable, to the ground contact of the inverter, see Figure 3.25. Thus, the input capacitance of the motor is considered. In the second test, the inverter feeds the motor using a simple open loop modulation technique. The measurements are compared with the simulations of the entire system, i.e. all three models discussed are connected together. Beside voltage

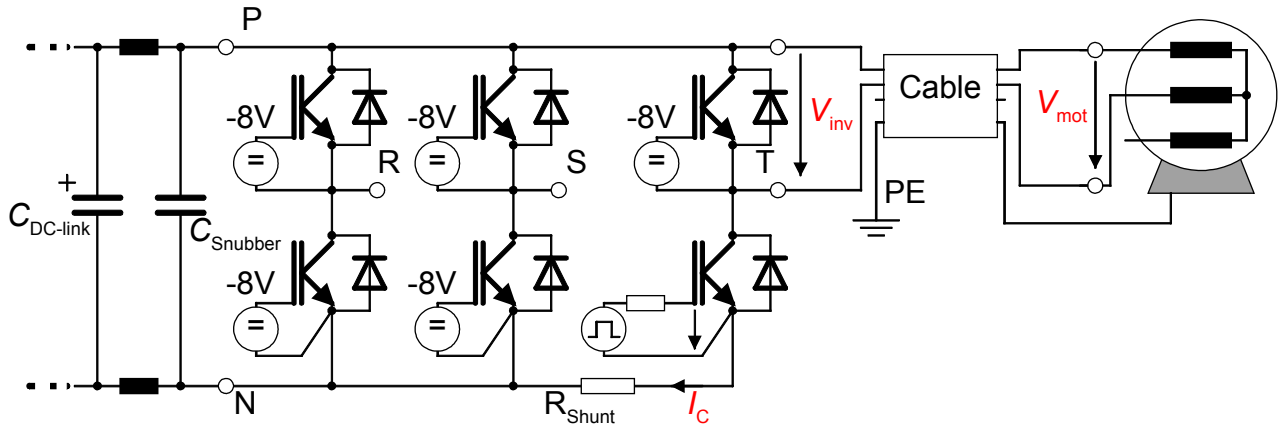


Figure 3.25: Test setup for measuring the reflections at motor terminals

reflections at the motor terminals, the common-mode ground current is measured and analyzed.

### 3.2.3.1 Effect of the input impedance of the motor

In the previous section, a large inductor was chosen as load to obtain a reflection coefficient  $K_L$  as high as possible, see Eq. 2.19 with the condition  $Z_L \gg Z_C$ . In this case, the motor impedance is smaller than the impedance of the load inductor and therefore, the reflection coefficient will be less. The input impedance of the motor will have also an effect on oscillation period  $T_{osc}$  of the reflections. Due to the high input capacitance, especially the stator winding – stator case capacitance, the traveling wave speed  $v_C = 1/\sqrt{L'C'}$  will be affected. This can be easily observed by comparing, for example, the wave reflection from Figure 3.26 (a) with the one from Figure 3.23 (a) (for LAPP cable:  $T_{osc} \approx 1.04 \mu s$  with load inductor and  $T_{osc} \approx 1.14 \mu s$  with motor). In Figure 3.26 (b), the same voltage reflection is plotted, this time using the full inverter to drive the motor. A common Space Vector modulation technique (SVPWM) was used to command the switches of the inverter. The motor speed was controlled using a simple open loop V/f characteristic. Same behavior and traveling wave characteristics are noticed in both cases.

Comparing now the voltage reflections from Figure 3.26 (b) and Figure 3.16 (b), a

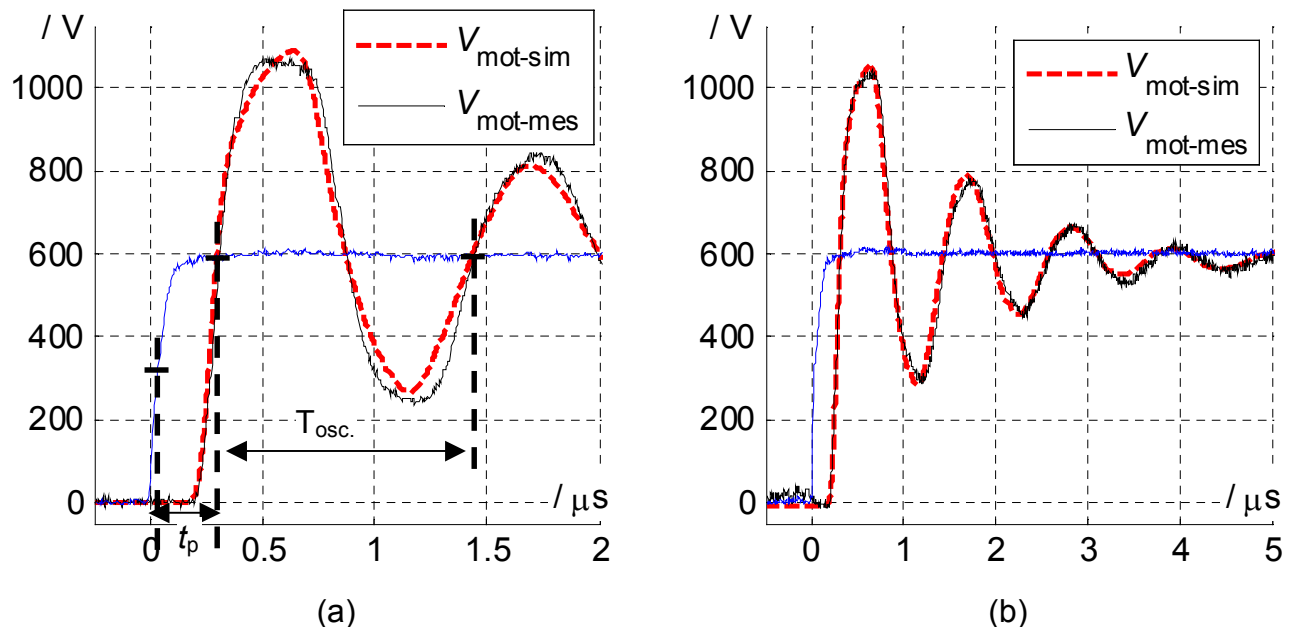


Figure 3.26: Voltage reflection at motor using buck converter topology (a) and motor operation (b)

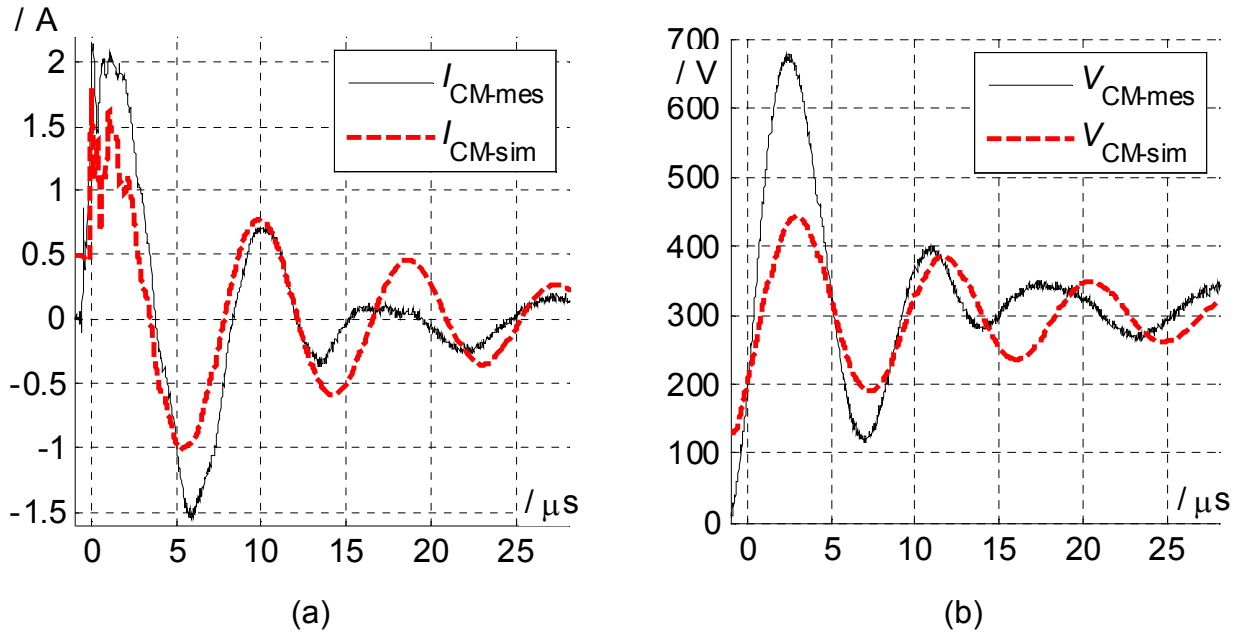


Figure 3.27: Measured vs. simulated CM ground current (a) and voltage (b) of the motor

bigger attenuation is observed when the motor is connected. As already mentioned, the input impedance of the motor is smaller than that of a single inductor, causing faster reduction of the reflections peaks (the 3<sup>rd</sup> peak is app. under 120% of the steady-state value, while for the load inductor case, the 4<sup>th</sup> peak fulfils this condition).

### 3.2.3.2 Common-mode voltage and ground current of the motor

In the motor simulation model, shown in Figure 2.35, the capacitive coupling between the stator winding and case is represented by two capacitances and damping resistors:  $C_{res1}$  and  $R_{res1}$  responsible for the high-frequency component of the CM current;  $C_{res2}$  together with  $R_{res2}$  determines the middle frequency oscillations, see Figure 3.27 (a). Due to the simplified motor model, the CM current peak is not precisely estimated; instead the oscillation period is roughly approximated. Improvements to this motor model are possible by adding additional ladder circuits, which replace the parameters  $C_{res1}$  and  $R_{res1}$ . They have been presented in [35], but they lead to a large increase of the complexity of the simulation. Therefore, these improvements will not be detailed here further. The simplified model, presented previously, will therefore be considered in further simulations, as it represents a good compromise between accuracy and simplicity.

In Figure 3.27 (b), the measured and simulated common-mode voltage  $V_{CM}$ , mainly responsible for the EDM bearing currents, is plotted. Same discrepancy is observed regarding the first peak, but oscillations are simulated more accurately. Overall, the simulations results are found to be satisfactory.

A second Siemens induction motor, for the same power range (4 kW) as the BBC motor (5 kW), was measured and modeled. The results and the measured characteristic of the input impedance vs. frequency are plotted for both common and differential modes in section 7.2.2 (Appendix).



## 4 Investigation of methods to reduce parasitic effects

Since the phenomena of overvoltage and motor bearing damage were directly related to the interference between fast switching inverter, long cables and motors, different methods to overcome these problems were studied intensively. Three major approaches may be distinguished:

→ methods related to inverters, where the voltage gradient at the inverter output is changed, by means of IGBT gate control or multi-level inverter topologies, so that the effect of the voltage reflections at the motor terminals is reduced [39]. Also, the common-mode voltage is reduced/eliminated using unconventional switching patterns [20];

→ methods related to cables, where additional filters are connected, either at the inverter output or at the motor terminals, to reduce the voltage slope, voltage overshoot and/or common-mode ground current [31];

→ methods related to motors, where additional measures, like stronger stator insulation or electrical isolated bearings etc., provide more motor immunity to the overvoltage stress or eliminate the destructive bearing currents [16].

The methods introduced above have their advantages or disadvantages and can be used simultaneously. Finally, it is always a question of application requirements vs. implementation costs, therefore the optimal compromise should always be found.

In this chapter, only the first two types of methods will be detailed, as the inverter and the cable were investigated thoroughly. The details, regarding the motor, were studied in a parallel work inside the DFG FOR575 research group [34]. Thus, the methods related to the inverter (regarding injection of unconventional voltage slopes and pre-/post-charge of cable's stray elements) are detailed in subchapters 4.1 and 4.2. The use of motor side and inverter output filters is further analyzed in 4.3 and 4.4.

### 4.1 Unconventional voltage slopes

#### 4.1.1 Increase of gate resistance $R_G$

The simplest way to reduce the voltage slope, influencing directly the switching behavior of the IGBT, is to reduce the gate current using larger gate resistances. As simple as it looks, this method is unpractical due to the high increase of the switching losses. To analyze the effect of the gate resistance in detail, the same configuration from section

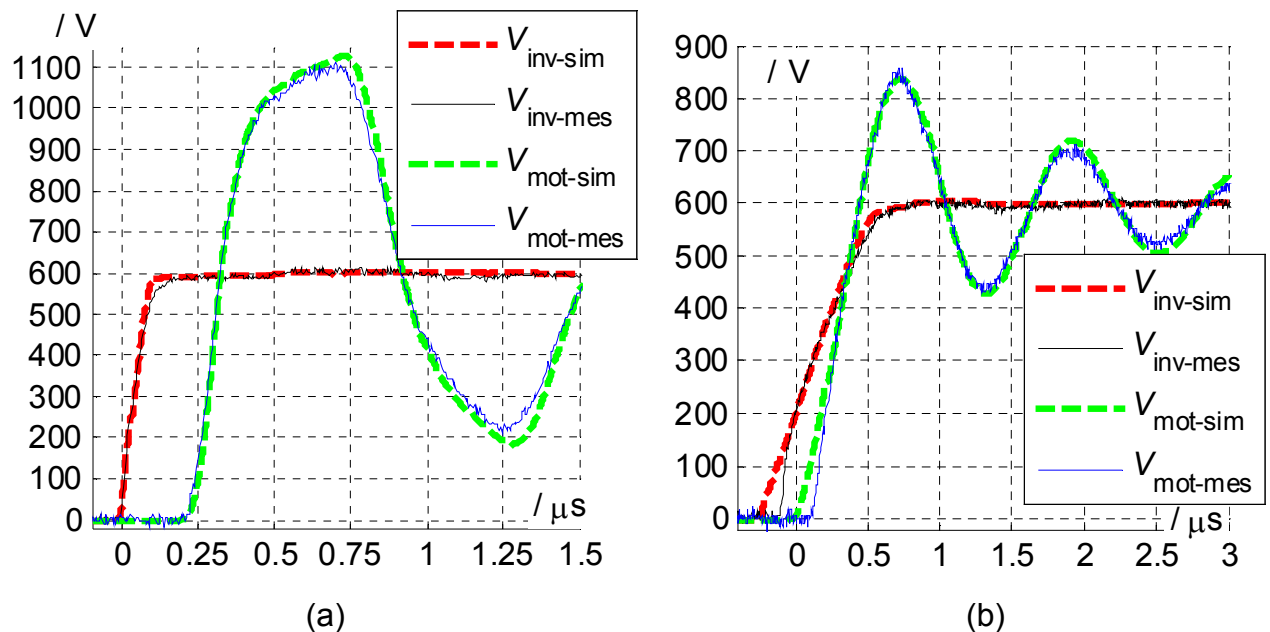
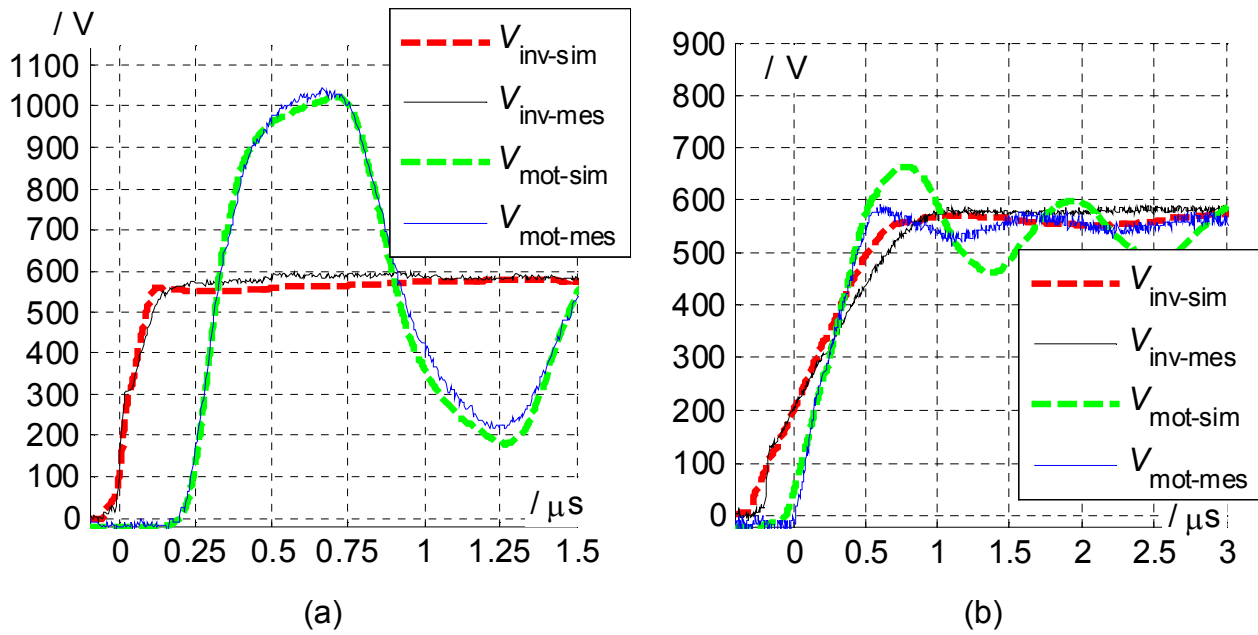


Figure 4.1: Voltages  $V_{inv}$  and  $V_{mot}$  during turn-on ( $I_c = 0A$ ) using  $R_G = 22\Omega$  (a) and  $R_G = 220\Omega$  (b)

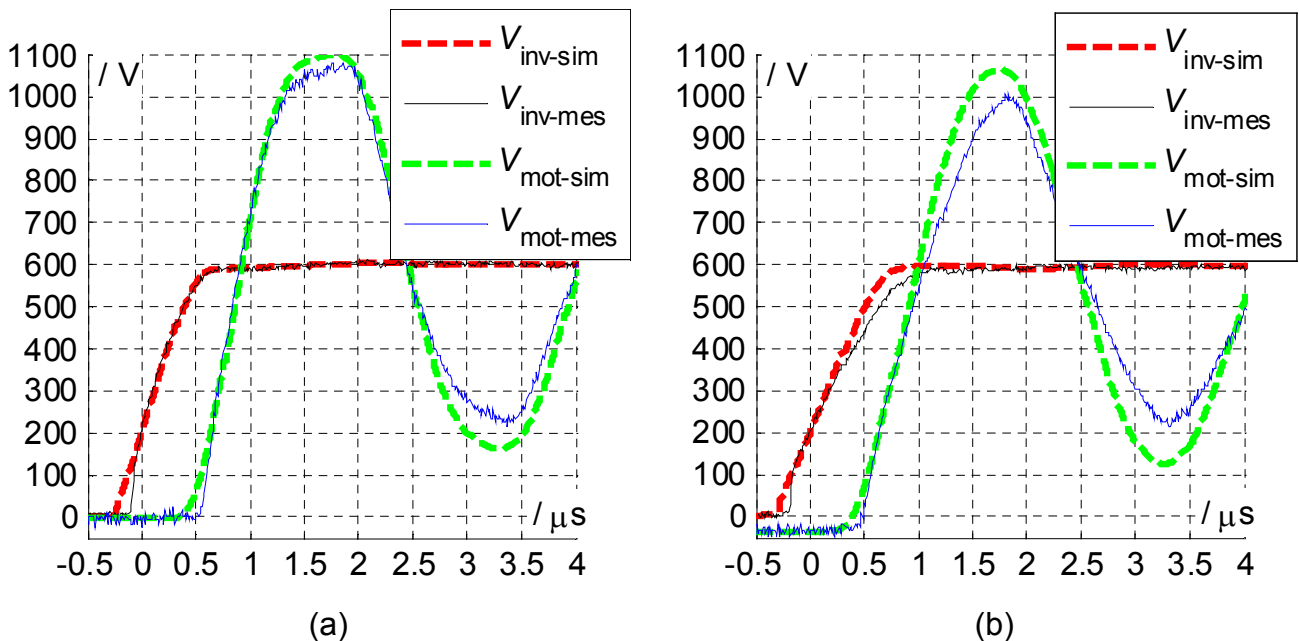


**Figure 4.2: Voltages  $V_{inv}$  and  $V_{mot}$  (turn-on + 34 m cable) at  $I_C = 36A$  for  $R_G = 22\Omega$  (a) and  $R_G = 220\Omega$  (b)**

3.2.3, see Figure 3.25, is used, i.e. buck-converter operation of the inverter only with the 3<sup>rd</sup> arm operating and a stator inductance as load. This setup is used with few switching pulses to avoid a thermal overload of the IGBT, due to the increased switching losses.

In Figure 4.1, the measurements and simulations of the inverter output voltage  $V_{inv}$  and motor terminals voltage  $V_{mot}$  are plotted together for the IGBT turn-on transient, using two gate resistance values  $R_G$ . It has to be considered that the plotted voltage  $V_{inv}$  represents actually the voltage across the freewheeling diode. While  $R_G = 22\Omega$  represents the optimal value, used in the data sheet to obtain the main characteristics, a ten times bigger value  $R_G = 220\Omega$  is used to significantly reduce the collector-emitter voltage slope  $dV_{CE}/dt$ . The voltage reflections are obtained using the shielded 34 m long cable, connected between inverter and motor. The mechanism can be described as follows:

- the high values of the gate resistance determine the reduction of the gate current level, mainly during Miller-Plateau phase. It was presented in Figure 2.11 (page 17) that, during this interval, the constant gate current charges the input capacitances of the IGBT and,



**Figure 4.3: Voltages  $V_{inv}$  and  $V_{mot}$  (turn on + 99 m cable) for  $R_G = 220\Omega$  at  $I_C = 0A$  (a) and  $I_C = 36A$  (b)**



together with  $C_{GC}$ , determines the voltage gradient. By simply reducing the current value, the voltage slope is reduced together with the voltage reflections at the motor terminals.

Additionally, the voltage gradient dependency on  $I_C$  was observed, especially at bigger gate resistance. In Figure 4.2, the same voltages are plotted (measured and simulated) during the turn-on transient of the IGBT, but at high stationary value of the collector current  $I_C = 35$  A. This difference was first noticed in subsection 3.2.1.2, see Table 3.3, and was found to be an effect of the charge-dependent diffusion capacitance  $C_{diff\_D}$ . Comparing both Figure 4.1 and Figure 4.2, it can be noticed that for  $R_G = 22 \Omega$  the difference in voltage gradients is having no effect on the voltage reflection, while  $R_G = 220 \Omega$  leads to significant voltage reflections at low stationary current  $I_C$ . This is possible due to the chosen cable length, i.e. the relation between the wave propagation time  $t_p$  and the voltage rise time  $t_r$ , see Eq. 2.29 and Eq. 2.30 from section 2.2.2. For a better overview, the values for  $t_r$ , depending on the gate resistance  $R_G$  and current  $I_C$  are listed in Table 4.1.

**Table 4.1: Voltage  $V_{inv}$  rise times dependent on  $R_G$  and  $I_C$  for LAPP and Ozoflex cable**

	$I_C = 0$ A				$I_C = 36$ A			
	$R_G = 22 \Omega$		$R_G = 220 \Omega$		$R_G = 22 \Omega$		$R_G = 220 \Omega$	
<b>34 m cable: <math>t_p \approx 220</math> ns</b>	mes.	sim.	mes.	sim.	mes.	sim.	mes.	sim.
$V_{inv}$ rise time $t_r$ / ns	96	79	604	629	144	114	968	863
$V_{mot}$ peak / V	1112	1127	856	838	1048	1024	592	663
<b>99 m cable: <math>t_p \approx 640</math> ns</b>	mes.	sim.	mes.	sim.	mes.	sim.	mes.	sim.
$V_{inv}$ rise time $t_r$ / ns	80	79	560	633	130	106	920	834
$V_{mot}$ peak / V	1096	1128	1080	1099	1048	1104	1008	1062

Concluding, the “worst-case” situation, regarding the peak of the voltage reflections during the IGBT turn-on transient, is found to be at low  $I_C$  current levels. If the 99 m long cable is connected between inverter and motor, the gate resistance should be much larger than  $220 \Omega$  to obtain a significant reduction of the voltage reflections. However, for technical reasons,  $R_G$  was not increased further as the switching losses increase too, leading to an unpractical burden for inverter. In Figure 4.3, the measured and simulated  $V_{inv}$  and  $V_{mot}$  are presented for the IGBT turn-on transient, when the 99 m long cable is connected, using  $R_G = 220 \Omega$  and considering the two different stationary  $I_C$  current levels: 0 A and 36 A. It can be observed that, only for  $I_C = 36$  A, the reduction effect on the voltage gradient is noticeable, i.e. the condition  $t_p < t_r$  is fulfilled; see also Table 4.1.

These observations are confirming the unpractical aspect of such measures in reducing the voltage reflections at the motor terminals; for switching losses measurements and estimations see Table 4.2. A different approach is therefore necessary and will be presented further.

#### 4.1.2 “2 Step Rise” voltage gradient

It is possible to significantly reduce the voltage reflections at the motor terminals by using unconventional voltage gradients (different than the constant ramp gradient). Such a voltage rise, called here “2 Step Rise”, consists in dividing the voltage slope in two equal parts and adding a dead time in the middle, where the voltage should remain constant. This method was introduced in [39] together with the derivation of the mathematical relations. The main idea is to inject two traveling voltage waveforms on the cable, which are time-shifted from each other. By controlling the shift period between the two injected waves, a significant reduction of the voltage reflections may be obtained.

Considering the transmission line model of the cable from section 2.2.1, the traveling voltage waves, from inverter to motor and back, are expressed using relations Eq. 2.17, Eq. 2.18, Eq. 2.20 and Eq. 2.22. After traveling four times between inverter and motor, the reflections will repeat with period  $4t_p$ . If the reflections at the motor and inverter side are

ideal, the wave will continue to reflect infinitely. In [39], the forward-traveling voltage is expressed separately from backward-traveling voltage. Both are calculated as a sum of all individual waves, traveling in the same direction and expressed as power series:

$$\begin{aligned}
 V_f(x, s) &= V_1(x, s) + V_3(x, s) + \dots = \\
 &= V(s) \cdot \left[ e^{\frac{x}{l} t_p \cdot s} + \left( K_S K_L \cdot e^{-2 t_p \cdot s} \right) \cdot e^{\frac{x}{l} t_p \cdot s} + \left( K_S K_L \cdot e^{-2 t_p \cdot s} \right)^2 \cdot e^{\frac{x}{l} t_p \cdot s} + \dots \right] = \\
 &= \frac{V(s) \cdot e^{\frac{x}{l} t_p \cdot s}}{1 - K_S K_L \cdot e^{-2 t_p \cdot s}};
 \end{aligned} \tag{Eq. 4.1}$$

$$\begin{aligned}
 V_b(x, s) &= V_2(x, s) + V_4(x, s) + \dots = \\
 &= V(s) \cdot K_L \cdot e^{-2 t_p \cdot s} \cdot e^{\frac{x}{l} t_p \cdot s} \left[ 1 + \left( K_S K_L \cdot e^{-2 t_p \cdot s} \right) + \left( K_S K_L \cdot e^{-2 t_p \cdot s} \right)^2 + \dots \right] = \\
 &= \frac{V(s) \cdot K_L \cdot e^{-2 t_p \cdot s} \cdot e^{\frac{x}{l} t_p \cdot s}}{1 - K_S K_L \cdot e^{-2 t_p \cdot s}}.
 \end{aligned} \tag{Eq. 4.2}$$

Thus, the total voltage at one point on the cable is obtained (Eq. 4.1 + Eq. 4.2):

$$V(x, s) = V_f(x, s) + V_b(x, s) = V(s) \cdot \frac{e^{\frac{x}{l} t_p \cdot s} + K_L \cdot e^{-2 t_p \cdot s} \cdot e^{\frac{x}{l} t_p \cdot s}}{1 - K_S K_L \cdot e^{-2 t_p \cdot s}}. \tag{Eq. 4.3}$$

If the variable  $x$  is defined ( $x = 0$  for inverter output and  $x = l$  for motor terminals), then the voltage can be calculated as follows:

$$V(0, s) = V(s) \cdot \frac{1 + K_L \cdot e^{-2 t_p \cdot s}}{1 - K_S K_L \cdot e^{-2 t_p \cdot s}}; \quad V(l, s) = V(s) \cdot \frac{(1 + K_L) \cdot e^{-t_p \cdot s}}{1 - K_S K_L \cdot e^{-2 t_p \cdot s}}. \tag{Eq. 4.4}$$

As already mentioned, to obtain a voltage cancellation at the motor terminals, two voltage waves are injected on the cable with half of DC-link amplitude and time shifted with  $\beta$ . In time domain, the voltage has the expression  $v_{2\text{Step}}(t) = [v(t) + v(t - \beta)] / 2$  and applying the Laplace transform, we get:  $V_{2\text{Step}}(s) = [V(s) + V(s) \cdot e^{-\beta \cdot s}] / 2$ . Now, inserting  $V(l, s)$  from Eq. 4.4, following expression is obtained [39]:

$$V_{2\text{Step}}(l, s) = V(s) \cdot \frac{1 + e^{-\beta \cdot s}}{2} \cdot \frac{(1 + K_L) \cdot e^{-t_p \cdot s}}{1 - K_S K_L \cdot e^{-2 t_p \cdot s}}. \tag{Eq. 4.5}$$

Representing the last term with a power series, the delay  $\beta$  can be combined with the exponential term, getting the following expression:

$$V_{2\text{Step}}(l, s) = V(s) \cdot \frac{1 + K_L}{2} \cdot \left[ e^{-t_p \cdot s} + e^{-(t_p + \beta) \cdot s} + K_S K_L \cdot e^{-3 t_p \cdot s} + K_S K_L \cdot e^{-(3 t_p + \beta) \cdot s} + \dots \right]. \tag{Eq. 4.6}$$

Inserting the condition  $\beta = 2 t_p$  in Eq. 4.6, the voltage  $V_{2\text{Step}}(l, s)$  is calculated:

$$V_{2\text{Step}}(l, s) = V(s) \cdot \frac{1 + K_L}{2} \cdot \left[ e^{-t_p \cdot s} + (1 + K_S K_L) \cdot e^{-3 t_p \cdot s} + K_S K_L (1 + K_S K_L) \cdot e^{-3 t_p \cdot s} + \dots \right],$$

and reducing the power series again, the final expression is obtained:

$$V_{2\text{Step}}(l, s) = V(s) \cdot \frac{1 + K_L}{2} \cdot \left[ e^{-t_p \cdot s} + \frac{(1 + K_S K_L) \cdot e^{-3 t_p \cdot s}}{1 - K_S K_L \cdot e^{-2 t_p \cdot s}} \right]. \tag{Eq. 4.7}$$

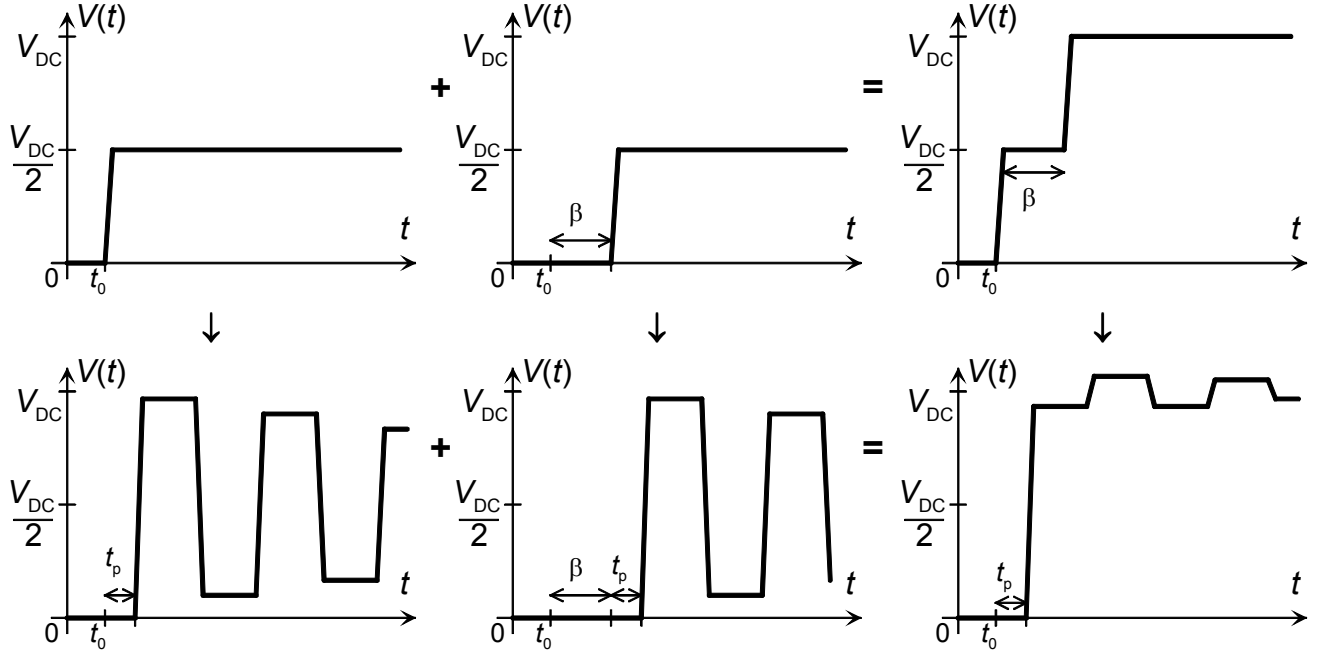


Figure 4.4: Graphic representation of the “2 Step Rise” method principle

Considering the ideal case, i.e. inverter  $\rightarrow$  short-circuit ( $K_S \approx -1$ ) and motor  $\rightarrow$  open-circuit ( $K_L \approx 1$ ), the voltage at the motor terminals, when the “2 Step Rise” method is applied, is approximately equal to the voltage at the inverter output, delayed only with the propagation time constant  $t_p$ . This leads to no reflections at the motor terminals:

$$V_{2\text{Step}}(l, s) \Big|_{K_S \approx -1, K_L \approx 1} \approx V(s) \cdot e^{-t_p \cdot s}.$$

Eq. 4.8

The effect of “2 Step Rise” method can be obtained also graphically, like Figure 4.4 shows. The two individual components of the voltage wave, injected to the cable, are represented on the top left and center part of the figure. The sum of them (top right part) will have the 2 Step shape with  $\beta$  delay between each wave. The effect of each individual voltage wave will be a voltage reflection at the motor terminals. It must be considered that each wave has  $V_{DC}/2$  amplitude and the reflection peak will therefore reach  $V_{DC}$  level. By comparing the two individual reflections, it can be noticed that, for  $\beta = 2t_p$ , they are shifted with  $180^\circ$  to each other, i.e. the peaks of first individual reflection overlap the valleys of the second one. By adding the individual reflections, the obtained total voltage wave presents small peaks due to the almost ideal characteristic of the reflection coefficients from motor and inverter considered in this case ( $K_S \approx -1$  and  $K_L \approx 1$ ).

To implement the “2 Step Rise” method, two different approaches are analyzed together with their advantages and disadvantages.

#### 4.1.2.1 “2 Step Rise” method implemented with unconventional gate driver

The unconventional gate driver circuits, also called active gate drivers, were studied before in [24] with the purpose of controlling the switching behavior of the IGBT by means of controlling the gate current. Thus, it is possible to control the gradients of current  $I_C$  or voltage  $V_{CE}$  by sensing these quantities, closing the control loop and comparing them with the user-defined reference values. The schematic of the active driver is drawn in Figure 4.5. The structure follows a classical control loop, with the IGBT as plant and the blocks, before the final amplification stage, as controllers. The state variables are the voltage and current gradients. Therefore, an external capacitor  $C_{dv}$  is used to sense the voltage gradient and an external stray inductor  $L_{dl}$  (or the internal stray inductance of the IGBT module between the auxiliary emitter pin and the main emitter pin) for sensing of the current gradient.

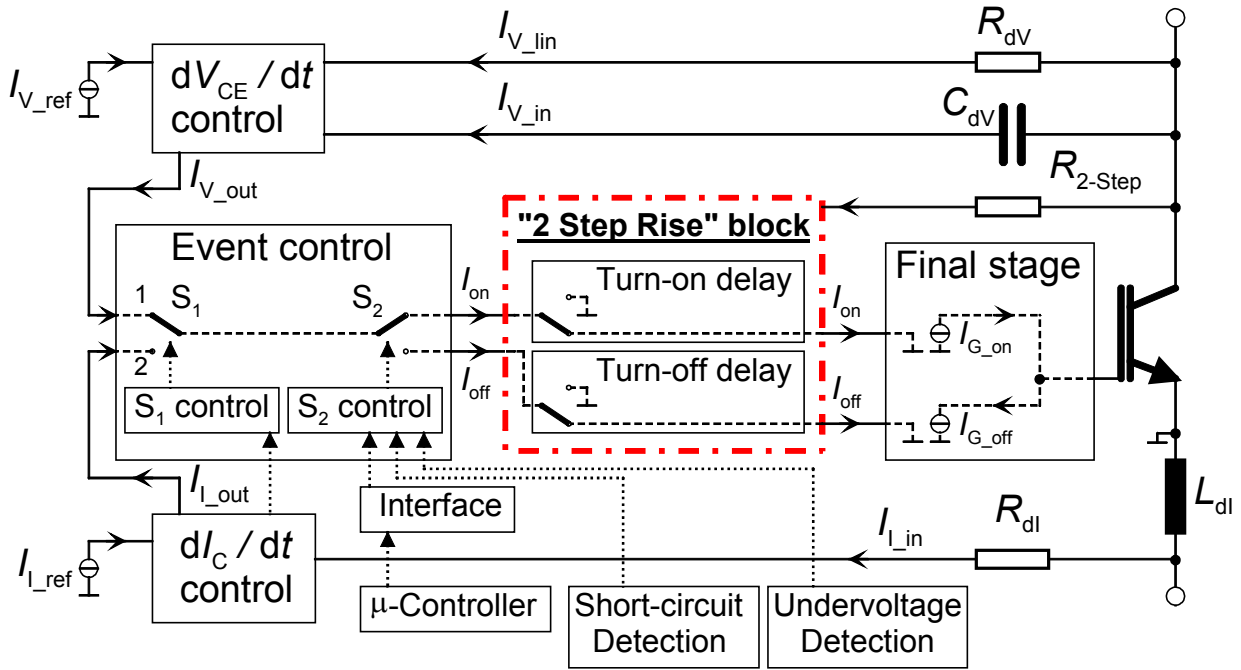


Figure 4.5: Block diagram of IGBT active gate driver with additional “2 Step Rise” block

The active driver is implemented using the current as a signal quantity and fast bipolar transistors, as the control loop should be fast as possible [24].  $C_{dv}$  delivers the current  $I_{V\_in}$  as a function of voltage gradient and  $R_{dv}$  delivers the current  $I_{V\_lin}$  dependent on the voltage  $V_{CE}$ . The latter is used for control linearization. The user can set the reference of the voltage gradient using  $I_{V\_ref}$ . The voltage gradient control block delivers  $I_{V\_out}$  at the output. In a dual way, the current gradient is measured with the stray inductance  $L_{dl}$  and then the voltage drop over this inductance is transformed in current ( $I_{I\_in}$ ) using  $R_{dl}$ . The reference  $I_{I\_ref}$  can be set by user and the output  $I_{I\_out}$  is fed further to the “Event Control” block. The two controls must run sequentially and not interfere during the turn-on and turn-off transitions. The switch  $S_1$  is responsible for this task and controlled directly by the control block for current gradient. If  $I_{I\_in}$  is greater than  $I_{I\_ref}$ , the switch  $S_1$  will commute to position 2 and the gate current is determined by  $I_{I\_out}$ . The switch remains on position 1 by default. Inside the “Event control” block there is a second switch  $S_2$ , which determines the type of transient (on or off) for IGBT. Therefore, this switch is connected to the  $\mu$ -controller through an interface. Additionally, the protection circuits, like short-circuit or undervoltage detection, may command directly this switch to turn-off in case of a failure.

The new feature, added to the active drive in this work, represents the “2 Step Rise” block, which is introducing the intermediate dead time when the voltage reaches  $V_{DC}/2$ . For that, the resistance  $R_{2-Step}$  is used to obtain the voltage-dependent current  $I_{2-Step}$ . The two IGBT transitions, separated by  $S_2$  in the previous block, are treated separately in this block also. When the current  $I_{2-Step}$  indicates the reach of the  $V_{DC}/2$  level, the switches of the two individual blocks will commute the current  $I_{on}$  or  $I_{off}$  to ground, thus interrupting the supply further to the “Final stage” block. By default, these switches are allowing the current  $I_{on}$  or  $I_{off}$  to flow further.

Finally, the currents for turn-on and turn-off transients are amplified and fed to/from the gate connection of the IGBT. Thus, adjusting the references  $I_{V\_ref}$  and  $I_{I\_ref}$ , the gate currents  $I_{G\_on}$  and  $I_{G\_off}$  are controlled independently to limit the  $I_C$  and  $V_{CE}$  gradients. However, the main focus in this work is to influence only the voltage gradient, therefore the current gradient will not be limited.

Using the active gate driver from Figure 4.5, the voltage slope can be reduced to fulfill the condition  $t_p < t_r$ , (see Eq. 2.29), i.e. a significantly reduction of the voltage overshoot at the motor terminals. However, because this approach is similar with the simple increase of

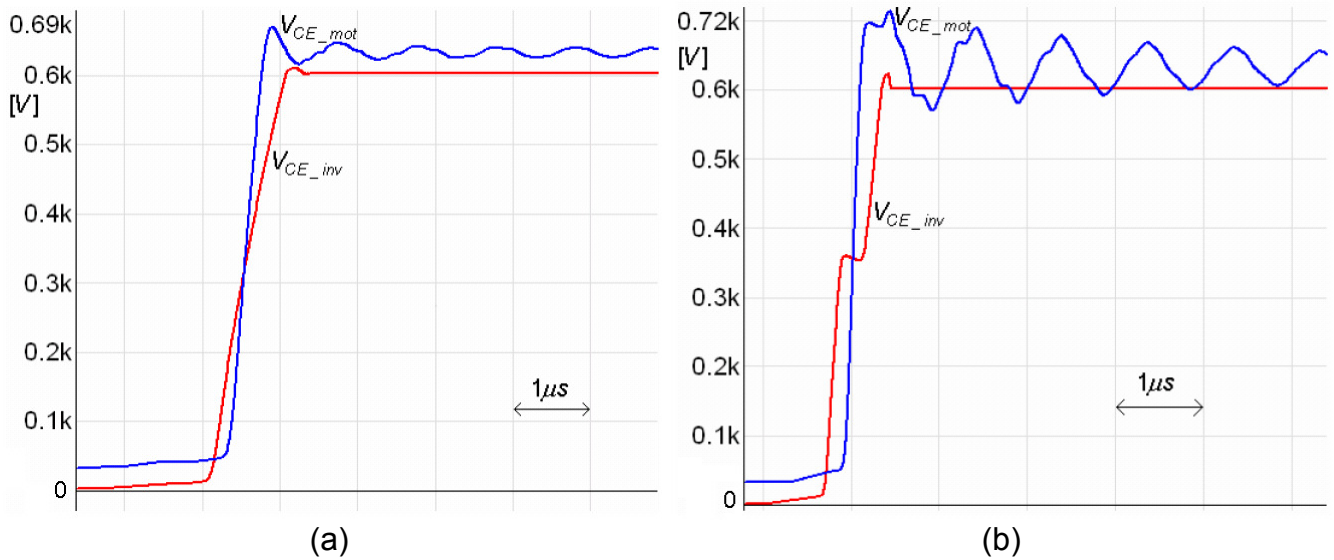


Figure 4.6: Simulated transient with decreased voltage slope (a) and "2 Step Rise" (b)

the gate resistance from section 4.1.1, this solution is not practical, due to the high increase of the switching losses. Using the "2 Step Rise" block, the "2 Step Rise" voltage slope can be obtained during the switching transient of the IGBT.

For example, the LAPP cable (34 m) is considered connected between inverter and load. The propagation time  $t_p$  is app. 220 ns and the delay for the voltage "2 Step Rise" is app. 440 ns, taking into consideration the condition  $\beta = 2t_p$  from the previous subsection. Further, Figure 4.6 shows the simulation results from [59] for the collector-emitter voltage  $V_{CE}$  and voltage reflection  $V_{mot}$  at the motor terminals during the IGBT turn-off transient. Comparison is made between the small voltage gradient (app. 600 V/ $\mu s$ , see Figure 4.6 (a)) and the "2 Step Rise" method (see Figure 4.6 (b)). Due to the high complexity of such a driver and lack of time for implementation and realization, only simulations were conducted. Available (external) simulation models were used to simulate the RF bipolar transistors. The effect of the "2 Step Rise" is clearly noticed when  $\beta$  is chosen 440 ns.

Table 4.2: Switching energy and overvoltage with large gate resistance and "2-Step rise" method

$dV_{CE}/dt \approx$	6 kV/ $\mu s$ ( $R_G = 22 \Omega$ )	0.6 kV/ $\mu s$ ( $R_G = 220 \Omega$ )	"2-Step Rise" method
Turn-On energy	1.2 mJ	12 mJ	7 mJ
Turn-Off energy	1.4 mJ	13 mJ	8 mJ
Voltage overshoot	app. 95%	< 15%	< 20%

Moreover, the energy was calculated for the considered switching transients and compared with the ones for different values of the gate resistance, see Table 4.2. Using

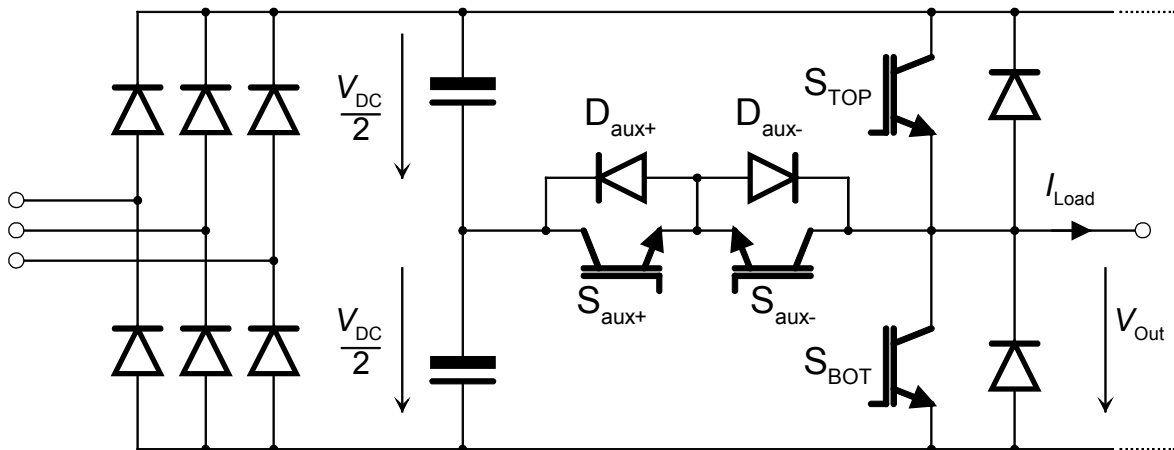


Figure 4.7: Three level inverter topology for "2 Step Rise" method implementation

the “2 Step Rise” method, 40% lower losses are obtained for approximately same voltage overshoot when compared to the  $R_G = 220 \Omega$  solution.

It can be noticed that the “2 Step Rise” method represents a good alternative for overvoltage reduction at the motor terminals. However, special attention must be taken due to the high increase of the switching losses. This aspect makes the implementation of the unconventional IGBT drivers rather complicated and feasible only for cables shorter than 30 m, where no large delay  $\beta$  is required between each individual voltage pulse [60].

#### 4.1.2.2 “2 Step Rise” method implemented with the three-level converter topology

A different approach, to impress the two voltage pulses on the cable with  $\beta$  delay, is the use of the three-level converters [39]. The usual voltage inverters for ASD are also called two-level inverters as they commute the output voltage between 0 and  $V_{DC}$ . If additional switches are connected to the mid point of DC link, the  $V_{DC}/2$  voltage level is available for commutation. A single leg from a three level inverter topology is shown in Figure 4.7. Additional switches,  $S_{aux+}$  and  $S_{aux-}$ , realize the connection between the DC-link mid point and inverter output, allowing the  $V_{DC}/2$  voltage level at the inverter output. Considering the

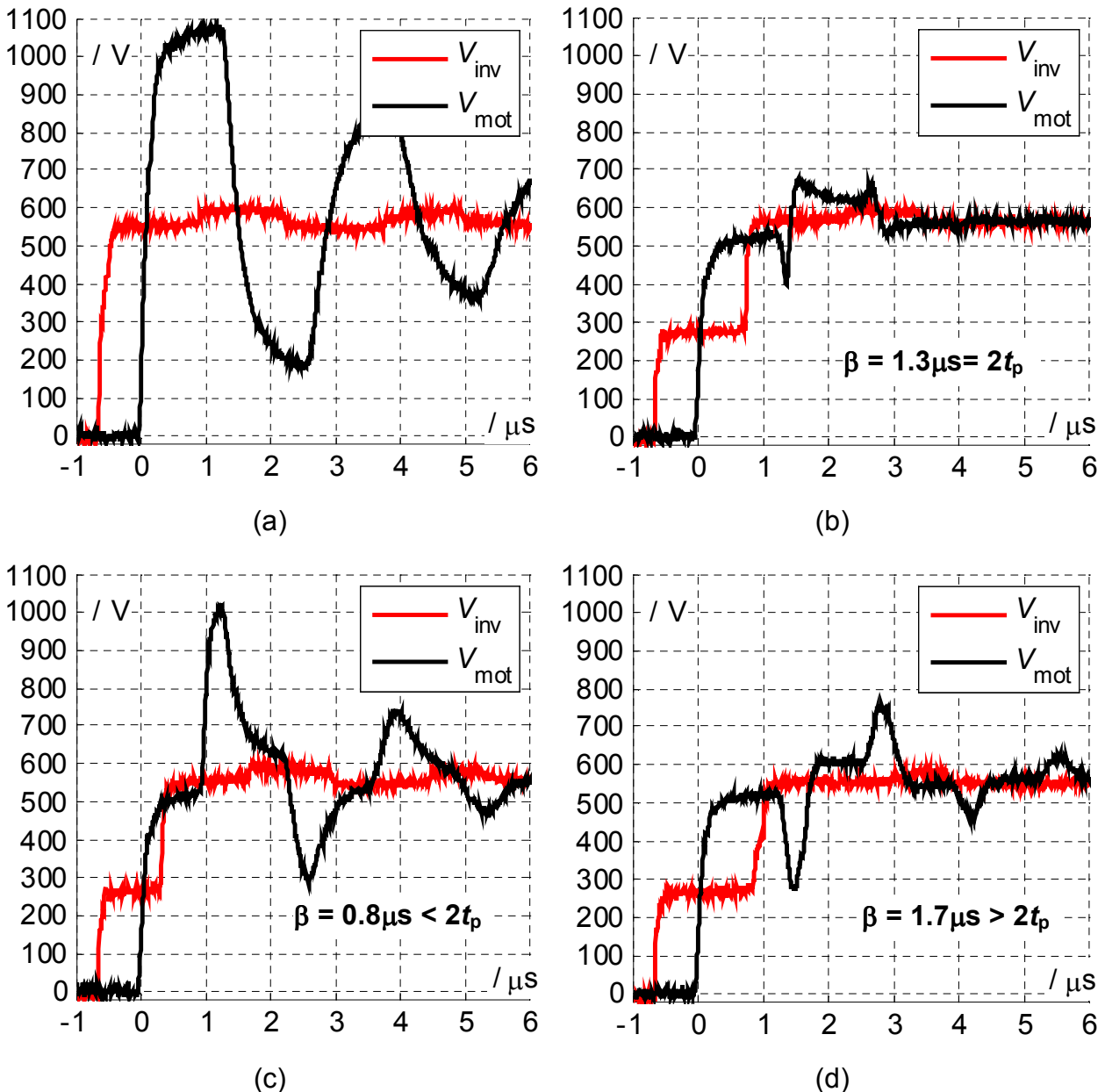


Figure 4.8: Measured voltage at inverter output and motor terminals using 3-level inverter topology

direction of the load current  $I_{Load}$  from Figure 4.7, the switching order is:  $S_{aux+}$  turns on first and the output voltage  $V_{Out}$  rises to  $V_{DC}/2$ ; the upper switch  $S_{TOP}$  turns on after time delay  $\beta$  and the output voltage rises further to the  $V_{DC}$  level. The anti-parallel diode  $D_{aux-}$  is used here to prevent a short-circuit of the upper DC-link capacitor. In a similar way but for negative load current values, the switch  $S_{aux-}$  is used to obtain the intermediate level  $V_{DC}/2$ . Finally, after  $S_{BOT}$  turns on the output voltage reaches the 0 level. Also here, diode  $D_{aux+}$  prevents the short-circuit of the lower capacitor from the DC link.

Such inverter topology was built and tested. If the auxiliary switches are also IGBTs, additional delays due to the switching transients make the use of this inverter topology unpractical for cable length shorter than 30 m. Therefore, the inverter prototype was connected to the 99 m long Ozoflex unshielded cable in order to obtain a clear view of the effect of the “2 Step Rise” method. Figure 4.8 presents the measurements obtained for different values of the  $\beta$  delay. When no intermediate step is applied to the  $V_{CE}$  gradient, the voltage reflections at the motor terminals with  $V_{peak} \approx 2 \cdot V_{DC}$  are observed; see Figure 4.8 (a). From Appendix, section 7.1.2, the wave propagation time is obtained from measurements:  $t_p \approx 650$  ns. According to condition  $\beta = 2 \cdot t_p$ , a necessary delay of  $1.3 \mu s$  is calculated. This can be noticed in Figure 4.8 (b), where the appropriate delay  $\beta$  leads to almost no voltage reflection at the motor terminals. If the intermediate step delay is smaller (approx.  $0.8 \mu s$  in Figure 4.8 (c)) or bigger (app.  $1.7 \mu s$  in Figure 4.8 (d)), the voltage reflection will increase.

In conclusion, the “2 Step Rise” method depends strongly on the cable length. For unknown lengths, the wave propagation must be first estimated from the wave reflections at the motor side and then the delay  $\beta$  calculated. This makes the application of this method an iterative process. Moreover, the “2 Step Rise” method can be implemented in two different ways but with corresponding costs: IGBT active drivers for short cable lengths (increase of switching losses) or three-level inverter topology for longer cables (increased inverter complexity and additional semiconductor switches).

## 4.2 Pre and post-charge of the cable stray elements

A second method, analyzed in this work, was first introduced in [10] and consists in applying a short pulse before and after each PWM pulse to pre and post-charge the stray inductances and capacitances of the cable. Because the traveling wave phenomenon consists in successive charging and discharging of the distributed capacitances and inductances along the cable length, it will be shown further that changing the initial conditions, leads to an elimination of the voltage reflections at the motor terminals.

This method starts with the analysis of the strongly-simplified HF equivalent circuit for motor and cable, namely a simple RLC circuit connected to a voltage source (DC-link circuit); see Figure 4.9 (a). The switches are ideal and commute the DC-link voltage  $V_{DC}$  at the inverter output. Thus, the line-line voltage will excite the RLC circuit starting with  $t_0$ . In this equivalent circuit, the capacitance  $C_{eq}$  includes the cable and motor capacitances while  $L_{eq}$  stands for the equivalent impedance of the cable. Additionally, the cable equivalent resistance  $R_{eq}$  may be considered, as the voltage reflections are eventually attenuated. After  $t_0$ , the voltage over the capacitance  $V_C$  will oscillate with period  $T_0$  and, depending on the  $R_{eq}$  value, will have an overshoot (response of a second order system). Applying KVL to the circuit from Figure 4.9 (a), following expression is obtained:

$$-V_{DC} + R_{eq} \cdot i_C(t) + L_{eq} \cdot \frac{di_C(t)}{dt} + v_C(t) = 0,$$

and, introducing the capacitor voltage  $V_C$  as a single unknown, the differential equation is:

$$L_{eq} C_{eq} \cdot \frac{d^2 v_C(t)}{dt^2} + R_{eq} C_{eq} \cdot \frac{dv_C(t)}{dt} + v_C(t) = V_{DC}. \quad \text{Eq. 4.9}$$

If the equivalent resistance of the cable is neglected then the condition for the worst case, regarding the wave oscillations, are obtained: a voltage overshoot app. twice the steady-state value ( $V_{DC}$  level); no oscillation attenuation. Therefore,  $R_{eq}$  will be neglected further and the solution for Eq. 4.9 will be:

$$v_C(t) = V_{DC} \cdot (1 - \cos \omega_0 t), \quad \text{Eq. 4.10}$$

where  $\omega_0$  represents the natural frequency in  $s^{-1}$  of the voltage wave. Applying the derivative to the equation Eq. 4.10, an expression for the capacitor current  $i_C(t)$  is obtained:

$$i_C(t) = C_{eq} \cdot \frac{dv_C(t)}{dt} = \frac{V_{DC}}{Z_{eq}} \cdot \sin \omega_0 t, \quad \text{Eq. 4.11}$$

with  $Z_{eq} = \sqrt{L_{eq} / C_{eq}}$ .

The condition for no reflections at cable end is stated in [10]: the energy for pre-pulse must not exceed the maximum value that allows the capacitance to charge up to the  $V_{DC}$  level. The maximum energy for the pre-pulse can, therefore, be defined as:

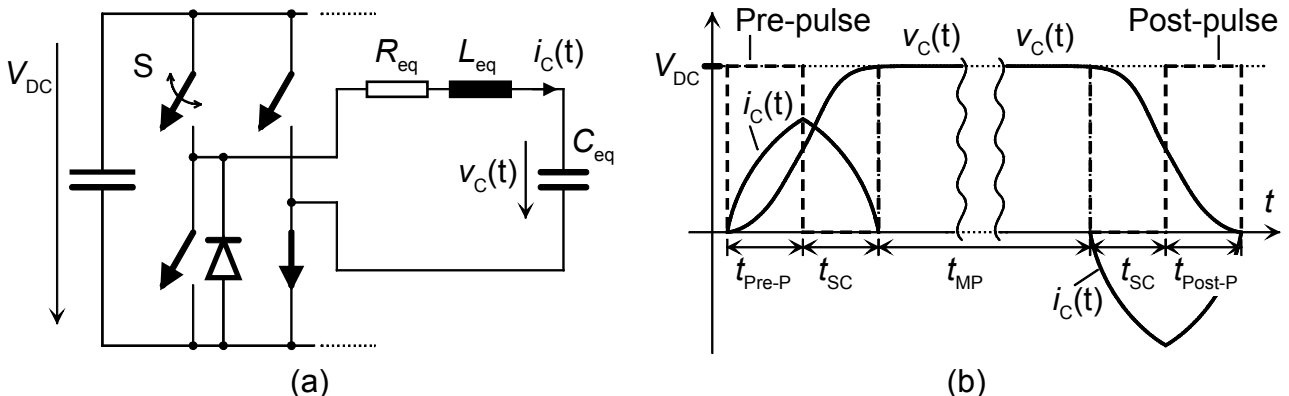


Figure 4.9: Equivalent circuit (a) and theoretical wave forms (b) for pre- and post-charge method



$$W_{\text{Pre-P,max}} = \frac{1}{2} \cdot C_{\text{eq}} \cdot V_{\text{DC}}^2. \quad \text{Eq. 4.12}$$

Considering the equivalent circuit from Figure 4.9 (a) and Eq. 4.11, the energy stored in the capacitor  $C_{\text{eq}}$  during the pre-pulse is:

$$W_{\text{Pre-P}} = \int_0^{t_{\text{Pre-P}}} V_{\text{DC}} \cdot i_C(t) = V_{\text{DC}}^2 \cdot C_{\text{eq}} \cdot (1 - \cos(\omega_0 \cdot t_{\text{Pre-P}})), \quad \text{Eq. 4.13}$$

where  $t_{\text{Pre-P}}$  represents the time duration of the pre-pulse. Comparing Eq. 4.13 and Eq. 4.12, this time interval is determined as a function of oscillation period  $T_0 = 1/f_0 = 2\pi/\omega_0$ :

$$0.5 \cdot C_{\text{eq}} \cdot V_{\text{DC}}^2 = C_{\text{eq}} \cdot V_{\text{DC}}^2 \cdot (1 - \cos(\omega_0 \cdot t_{\text{Pre-P}})) \Rightarrow t_{\text{Pre-P}} = (1/6) \cdot T_0. \quad \text{Eq. 4.14}$$

During  $t_{\text{Pre-P}}$ , the voltage  $v_C$  and current  $i_C$  rise, while the energy is stored in both inductor  $L_{\text{eq}}$  and capacitor  $C_{\text{eq}}$  from the equivalent circuit. A short-circuit period  $t_{\text{SC}}$  must follow the pre-pulse period to allow the inductor pass its energy further to the capacitor. During this time interval, the voltage source  $V_{\text{DC}}$  is short-circuited and  $t_{\text{SC}}$  should be equal

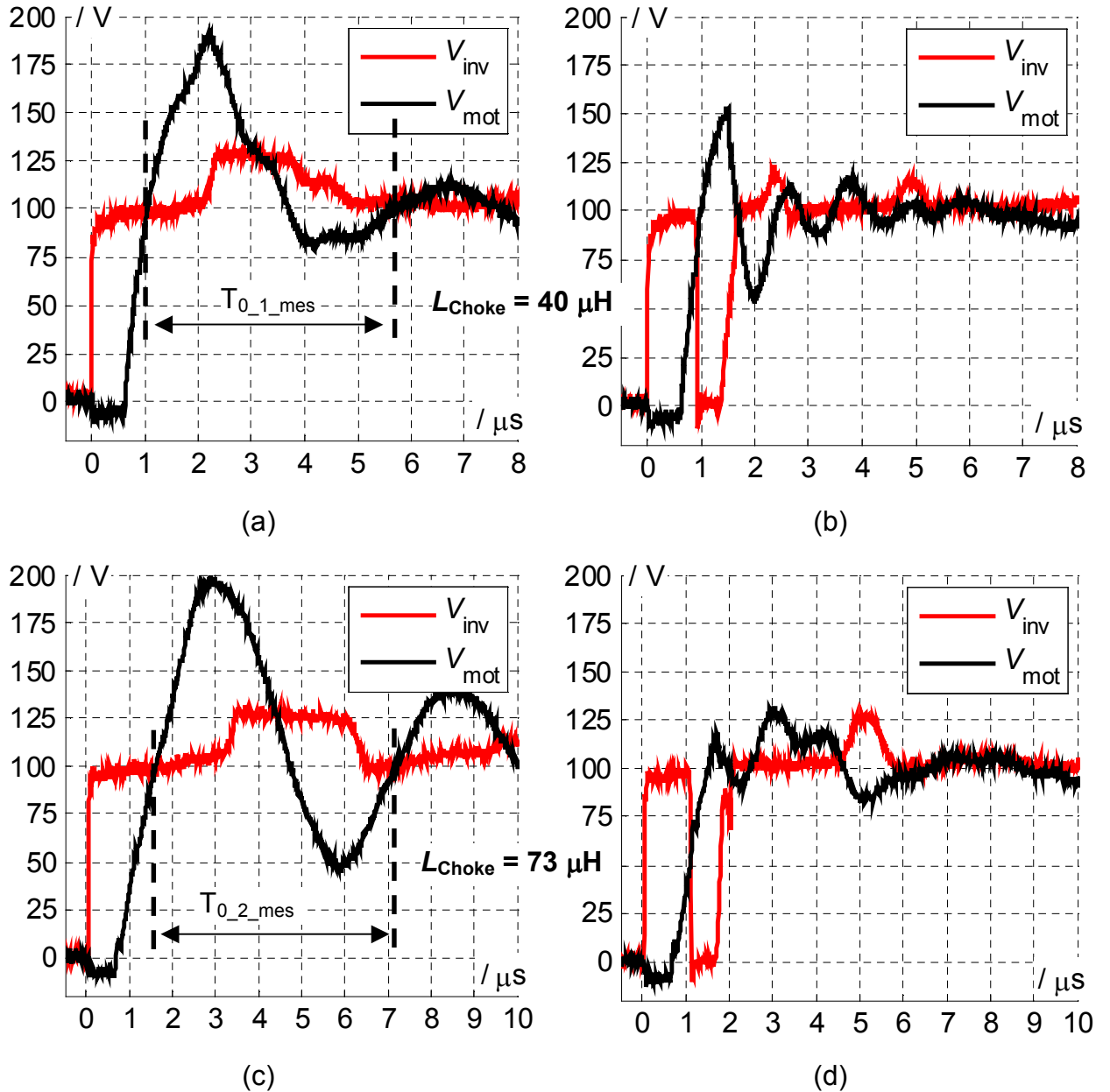


Figure 4.10: Measured voltage at inverter output and motor terminals using pre-charge method

to  $t_{\text{Pre-P}}$  in order to reduce  $i_C$  back to zero, see Figure 4.9 (b). The capacitor voltage  $v_C$  will increase further, during the short-circuit period, to the  $V_{\text{DC}}$  level. Thus, at the end of  $t_{\text{SC}}$ , the main pulse may occur, having the capacitances of cable and motor loaded at the  $V_{\text{DC}}$  voltage level, and in ideal case no voltage reflections occur.

In Figure 4.9 (b), the pulses before and after the main pulse are shown together with the theoretical waveforms for the capacitor current  $i_C$  and voltage  $v_C$ . It can be noticed that a similar procedure must be followed at the end of the main pulse (IGBT turn-off transient) but this time in reverse direction: first, a short-circuit state is applied, during the  $t_{\text{SC}}$  time interval, to decrease the voltage  $v_C$  (passing a part of the energy to the inductor  $L_{\text{eq}}$ ); second, the post pulse is applied during the  $t_{\text{Post-P}}$  period. If such a procedure is not used, the energy will bounce between  $L_{\text{eq}}$  and  $C_{\text{eq}}$ , in form of oscillations at both begin and end of the main pulse, until  $R_{\text{eq}}$  damps these oscillations.

The measurements were carried out at a small setup, as special adjustments to normal PWM modulation are necessary. A FPGA logic unit was used to deliver the switching instants for the pre- and post-pulses. This unit allows a good time resolution (faster clock than the CPLD unit from the AML board) and, hence, the possibility of a fine tuning of the

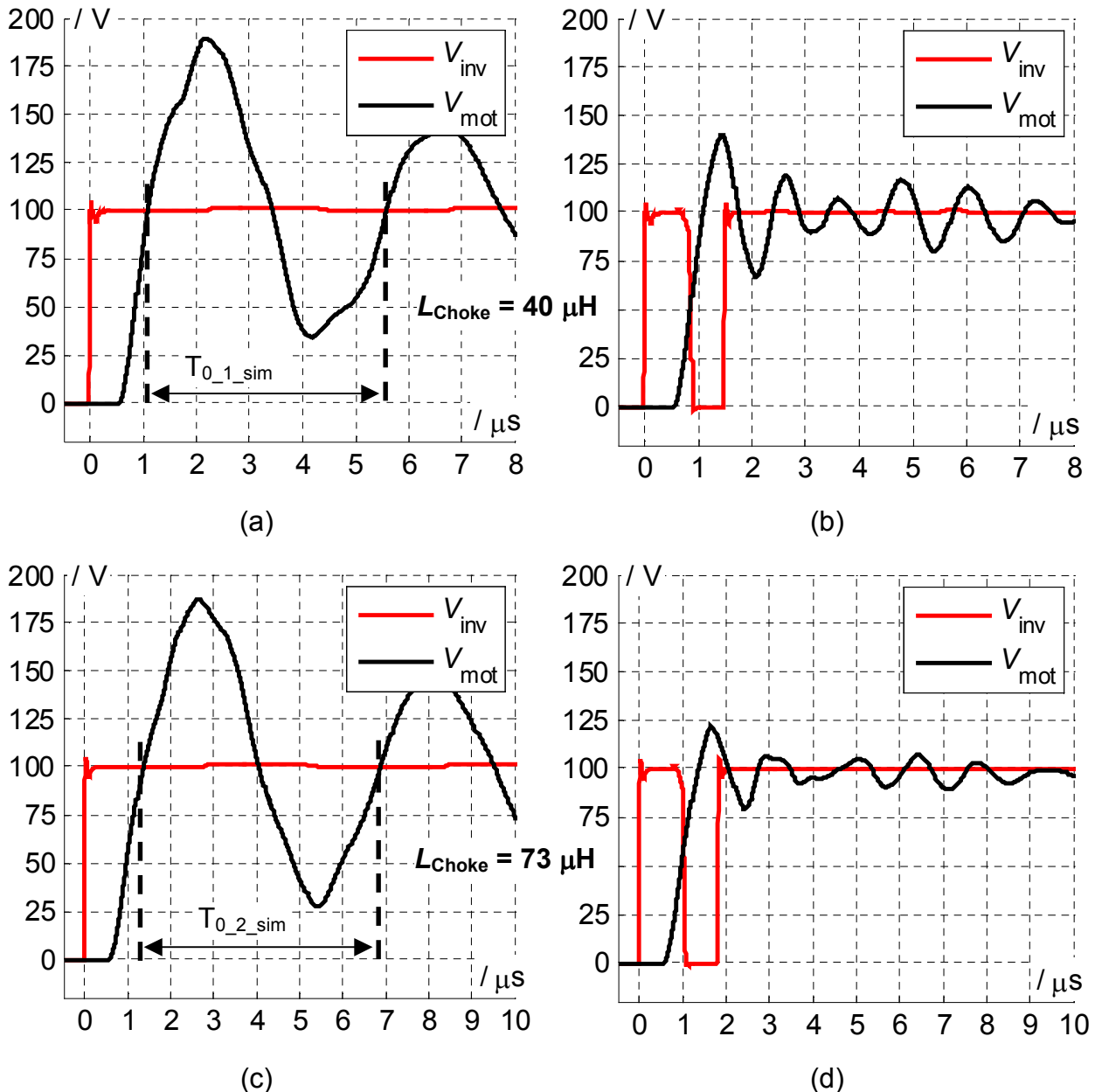


Figure 4.11: Simulated voltage at inverter output and motor terminals using pre-charge method

time intervals  $t_{\text{Pre-P}}$ ,  $t_{\text{SC}}$  and  $t_{\text{Post-P}}$ . Also, smaller DC-link voltage levels were preferred to bigger ones due to safety reasons (100 V instead of 560 V). However, the effect of the pre- and post-charge method remains unaltered for the smaller DC-link voltages.

During the measurements, following disadvantage was noticed: pre- and post-charge method does not work without an inverter output choke. The strongly simplified equivalent circuit fails in case of distributed cable parameters, i.e. the equivalent inductor  $L_{\text{eq}}$  from Figure 4.9 (a) is no longer available directly at inverter the output and before the equivalent capacitor  $C_{\text{eq}}$ . That is why this method works only with inverter output chokes. Moreover, the authors from [10] recommend this method in order to reduce the necessary output chokes and to obtain the same voltage overshoot at the motor side.

Figure 4.10 shows the measured line-line voltages at the inverter output and motor terminals for two different values of output chokes. In Figure 4.10 (a) and (b) a 40  $\mu\text{H}$  output inductor was used. The effect of the pre-pulse can be seen in figure (b) where a voltage overshoot of app. 50% is still noticed. When no pre-pulse is applied, Figure 4.10 (a), the voltage overshoot is high and the wave oscillation on the cable is  $T_{0\_1\_mes} \approx 4.6 \mu\text{s}$ . According to Eq. 4.14, the following time interval is calculated  $t_{\text{Pre-P}_1} = t_{\text{SC}_1} \approx 766 \text{ ns}$ . Figure 4.10 (c) and (d) shows the same measurements but with 73  $\mu\text{H}$  output choke. The voltage overshoot is under 25% in this case, figure (d), while the oscillation period  $T_{0\_2\_mes} \approx 5.6 \mu\text{s}$ , see figure (c), leads to a time interval  $t_{\text{Pre-P}_2} = t_{\text{SC}_2} \approx 933 \text{ ns}$ .

The connection between the inverter prototype and inductive load was realized using the 99 m Ozoflex cable. Comparing the obtained time intervals, necessary for pre- and post-charge method, with the wave propagation delay for this cable ( $t_p \approx 650 \text{ ns}$ ) it can be noticed, that only for  $t_{\text{Pre-P}} > t_p$ , the presented method will have an effect on overvoltage, otherwise the wave propagation delay will be dominant.

Similar results were obtained from simulations, presented in Figure 4.11. For the 40  $\mu\text{H}$  inverter output choke, the results are shown in Figure 4.11 (a) and (b) without and with pre-charge method, respectively. The oscillation period  $T_{0\_1\_sim} \approx 4.5 \mu\text{s}$  is close to the measured one. The 73  $\mu\text{H}$  output choke leads to the results from Figure 4.11 (c) and (d), with an oscillation period  $T_{0\_2\_sim} \approx 5.51 \mu\text{s}$ , also closed to the measured value. The same tendency from measurements is observed in simulations too, namely the use of inverter output chokes is limited by the condition  $t_{\text{Pre-P}} > t_p$ . The 40  $\mu\text{H}$  choke determines smaller pre-pulse and short-circuit times (closed to the wave propagation delay) than the 73  $\mu\text{H}$  choke, thus the voltage overshoot will be higher (app. 45%).

Finally, it can be concluded that the pre- and post-charge method represents a good solution only in combination with inverter output chokes. Using solely output chokes, the oscillations are damped e.g. by the parallel connected resistances. Applying pre-charge pulse, the oscillations are damped by increasing the voltage across the cable capacitance to the  $V_{\text{DC}}$  level, before applying the main pulse. But the switching losses are increasing three times as for each main pulse two additional pulses are required. Therefore, the fast switching devices, like MOSFETs, are preferred in this case.

Using the developed simulation models for inverter, cable and motor, a good estimation of the voltage oscillations is achieved, see measured / simulated pairs ( $T_{0\_1\_mes} / T_{0\_1\_sim}$ ) and ( $T_{0\_2\_mes} / T_{0\_2\_sim}$ ). Based on this estimation, the appropriate time intervals  $t_{\text{Pre-P}}$  and  $t_{\text{SC}}$  are directly calculated. Finally, the results obtained from measurements and simulations are in good agreement.

### 4.3 Use of cable terminators

Several methods for the overvoltage reduction, dealing with different inverter topologies and switching strategies, were analyzed in the previous two subchapters. In this and next subchapter, the main focus will shift to the cable and the overvoltage reduction methods dealing with the cable. The filters are of large use nowadays in industry due to their simplicity. However, many aspects must be regarded when filters are introduced in the inverter-cable-motor systems. The major aspect represents the filter losses, which will affect the overall efficiency of the system. Moreover, supplementary costs are involved, too, as passive elements of a high quality, especially the inductors, come together always with higher costs. Therefore, an analysis and finally a comparison of the mostly used filters in industry will be further given, starting with the simplest ones, the motor terminals filters also known as cable terminators, and ending with the inverter output filters.

On one hand, the cable terminators are based on a different operation principle as the inverter output filters, namely the voltage overshoot is reduced when the cable impedance is matched with the help of the additional filter impedance. On the other hand, the inverter output filters are affecting the voltage gradient at the inverter output, thus allowing milder voltage slopes to be impressed to the cable.

#### 4.3.1 Termination resistances

The simplest cable terminators can be implemented only with resistances. This approach is widely spread in communication, where resistive terminators are avoiding the signal reflections at the receiving side when the line impedance is matched. Usual values for such resistances are varying between 50  $\Omega$  and 100  $\Omega$ , depending mostly on the type of the cable. For example, the 50-Ohm resistances are well suited for the coaxial cables used in the 100 Base-T computer networks.

While in the communication domain low voltages are used (in range of tens to few volts), the voltages applied at the inverter output are much larger (above 300 V) in ASD, which makes the use of the resistive cable terminators very unpractical due to the high losses. However, this type of terminator was investigated only for comparison purposes.

Figure 4.12 illustrates the topology of this terminator, where the resistances can be connected in a Y or  $\Delta$  configuration. Thus, the necessary resistance values, matching the cable impedance, will depend on the configuration. For example, the 34 m long shielded cable is considered. For the Y connection, the corresponding cable impedance is app. 35  $\Omega$  (common-mode impedance  $Z_{Cab\_CM}$ ) while for the  $\Delta$  connection the differential mode impedance  $Z_{Cab\_DM}$  is app. 110  $\Omega$  (see Table 7.3 from section 7.1.1). Using the similar values for the filter resistances, the voltage overshoot at motor terminals is damped. The simulations are presented for the Y filter configuration and two resistance values in Figure 4.13:  $R_{F\_Y} = Z_{Cab\_CM}$  in Figure 4.13 (a) and  $R_{F\_Y} = 2 Z_{Cab\_CM}$  in Figure 4.13 (b). It can be

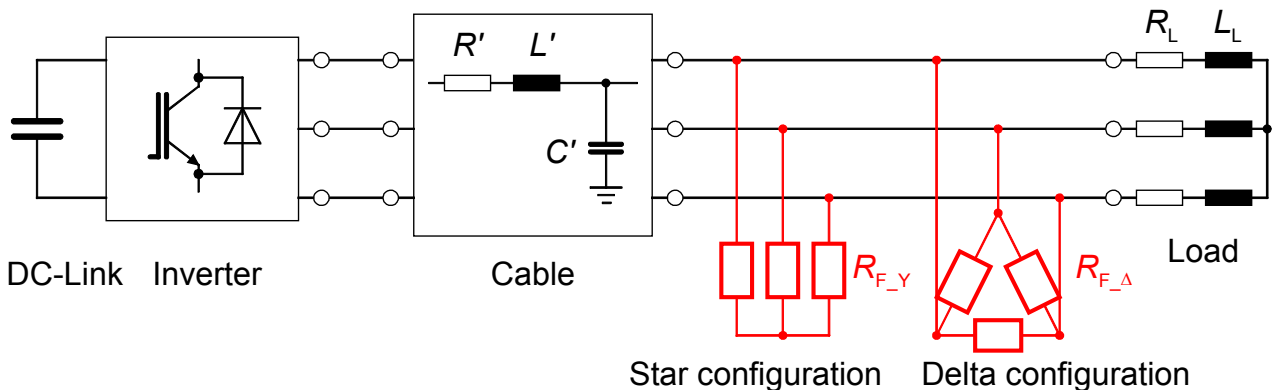


Figure 4.12: Star (Y) and delta ( $\Delta$ ) configurations for resistive cable terminator

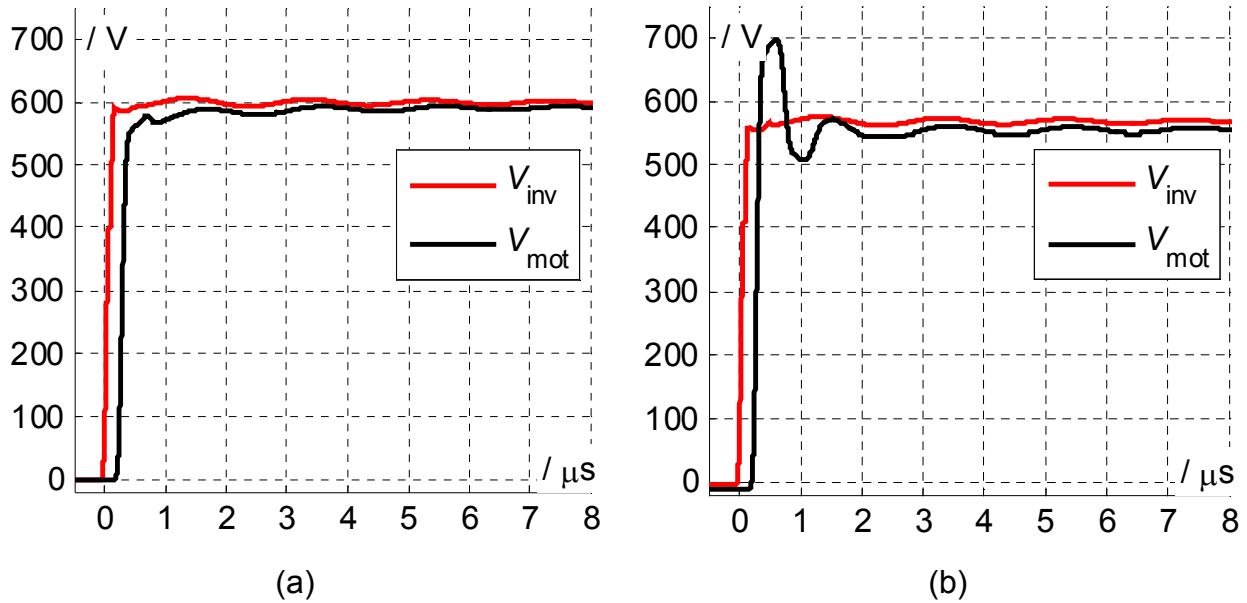


Figure 4.13: Simulated line-line voltage at motor terminal for  $R_{F\_Y} = Z_{CM}$  (a) and  $R_{F\_Y} = 2 Z_{CM}$  (b)

noticed that, for higher resistance values, the oscillations are no longer 100% damped and a voltage overshoot of app. 22% is obtained.

The resistive losses of the terminator were calculated from simulations and the results are summarized in Table 4.3 for both Y and  $\Delta$  configurations and the two different values of the  $R_F$  resistance.

Table 4.3: Estimated losses for resistive cable terminator

	Star (Y) configuration	Delta ( $\Delta$ ) configuration
$R_F = Z_{Cab\_CM/DM}$	Losses: 3070 W Overshoot: none	Losses: 2650 W Overshoot: none
$R_F = 2 \cdot Z_{Cab\_CM/DM}$	Losses: 1411 W Overshoot: 22%	Losses: 1350 W Overshoot: 24 %

### 4.3.2 RC filters

A better alternative to the simple resistive terminators is the RC-filter, consisting in a series connection of resistance and capacitance. Like in the previous case, two configurations are possible, namely the Y and  $\Delta$  configurations. The resistances alone damp the voltage overshoot but capacitances cut off the fundamental DC-component of the current through resistances, thus reducing the losses considerably. Both star (Y) and

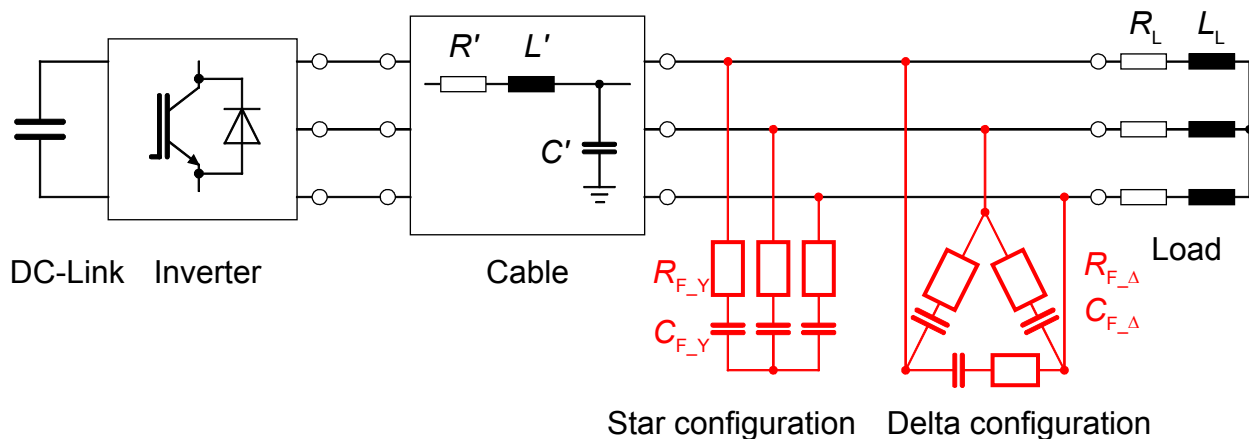
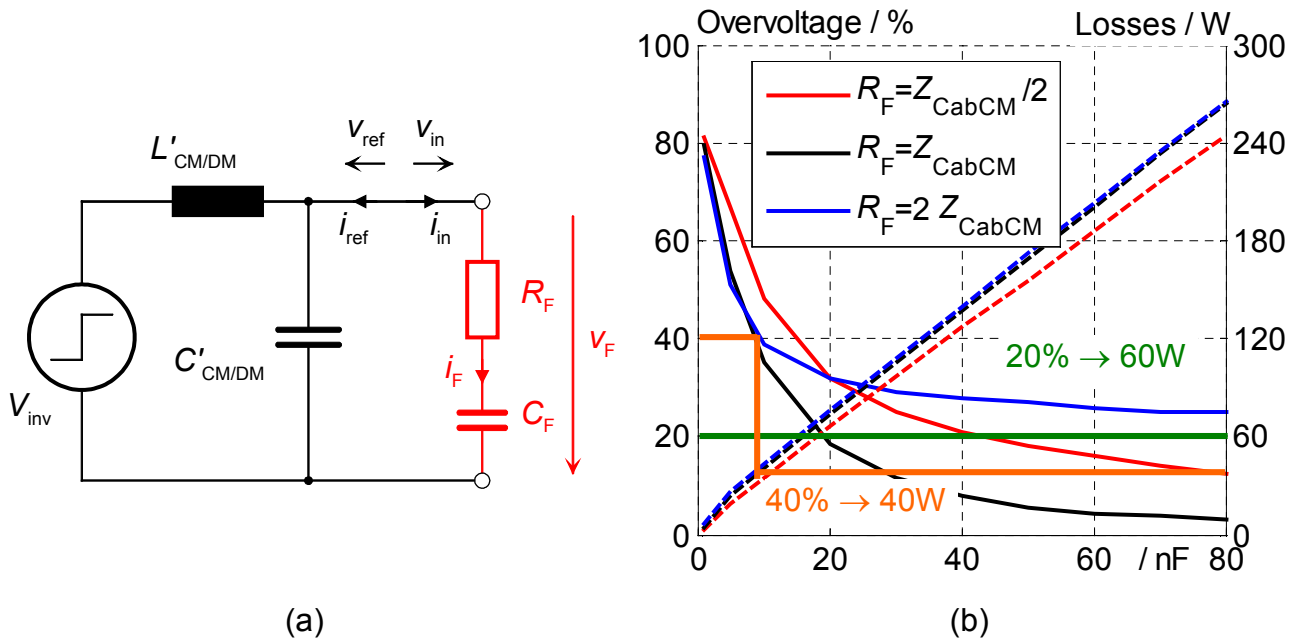


Figure 4.14: Y and  $\Delta$  configurations for RC cable terminator



**Figure 4.15: Equivalent circuit for RC filter design (a); Overvoltage (solid) and losses (dashed) vs.  $R_F$  and  $C_F$  characteristics (b)**

delta ( $\Delta$ ) connections for the RC filters are shown in Figure 4.14. The most important issue for implementing a filter is to calculate the parameters of the filter. A design algorithm is presented in [31], which relies on the strongly-simplified equivalent circuit of the inverter-cable system from Figure 4.15 (a). In this figure, the cable parameters have to be adjusted, depending on the type of filter configuration: CM for the Y connection or DM for the  $\Delta$  connection. Further, the star (Y) connection will be considered for exemplification.

The incident and the reflected voltage ( $v_{in}$  and  $v_{ref}$ ) together with the current ( $i_{in}$  and  $i_{ref}$ ) waves are connected by the cable impedance  $Z_{Cab\_CM}$ , using following relations:

$$v_{in} = Z_{Cab\_CM} \cdot i_{in}; \quad v_{ref} = Z_{Cab\_CM} \cdot i_{ref}. \quad \text{Eq. 4.15}$$

The voltage at the terminals of the filter is:

$$v_F = v_{in} + v_{ref}; \quad i_F = i_{in} - i_{ref}. \quad \text{Eq. 4.16}$$

The differential equation for the filter is expressed with:

$$v_F = R_F \cdot i_F + \frac{1}{C_F} \cdot \int i_F \cdot dt. \quad \text{Eq. 4.17}$$

Inserting Eq. 4.15 and Eq. 4.16 in Eq. 4.17, the following expression is obtained:

$$v_{in} + v_{ref} = R_F \cdot \left( \frac{v_{in}}{Z_{Cab\_CM}} - \frac{v_{ref}}{Z_{Cab\_CM}} \right) + \frac{1}{C_F} \cdot \int \left( \frac{v_{in}}{Z_{Cab\_CM}} - \frac{v_{ref}}{Z_{Cab\_CM}} \right) \cdot dt, \quad \text{Eq. 4.18}$$

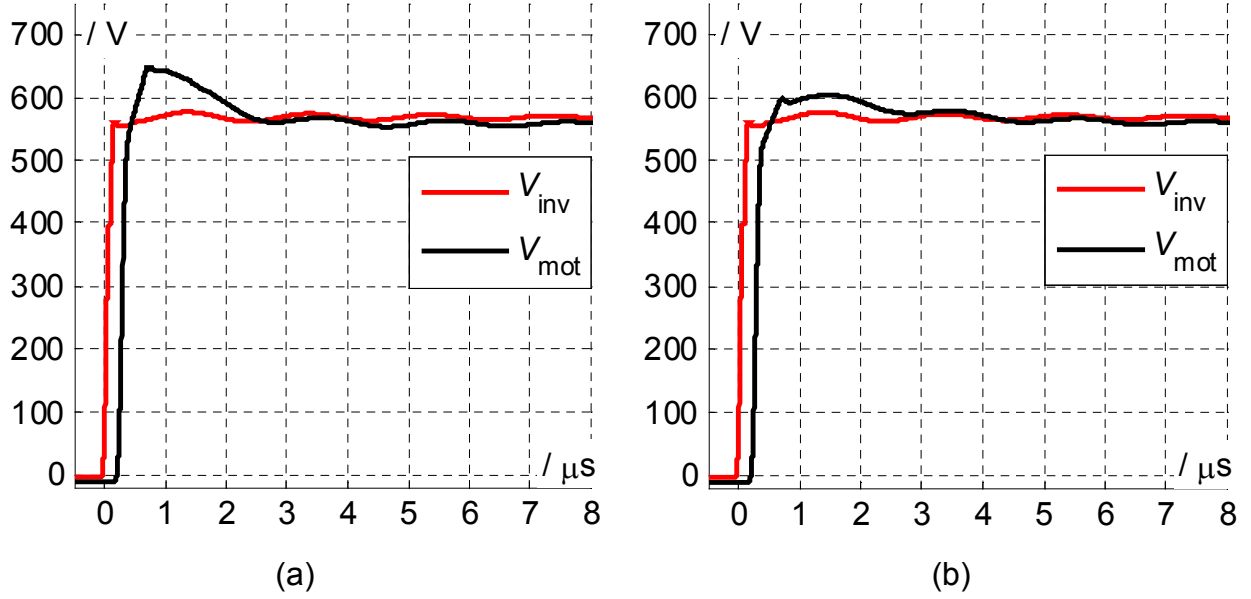
which can be rearranged with  $v_{ref}$  at the left side in the following way:

$$\begin{aligned} (R_F + Z_{Cab\_CM}) \cdot v_{ref} + \frac{1}{C_F} \cdot \int v_{ref} \cdot dt &= (R_F - Z_{Cab\_CM}) \cdot v_{in} + \frac{1}{C_F} \cdot \int v_{in} \cdot dt \quad \left| \frac{d}{dt} \Rightarrow \right. \\ \Rightarrow (R_F + Z_{Cab\_CM}) \cdot \frac{dv_{ref}}{dt} + \frac{v_{ref}}{C_F} &= (R_F - Z_{Cab\_CM}) \cdot \frac{dv_{in}}{dt} + \frac{v_{in}}{C_F}. \end{aligned} \quad \text{Eq. 4.19}$$

Further, the incident voltage wave is considered constant  $v_{in} = V_{DC}$  (i.e.  $dv_{in}/dt = 0$ ) and the differential equation from Eq. 4.19 becomes:

$$(R_F + Z_{Cab\_CM}) \cdot \frac{dv_{ref}}{dt} + \frac{v_{ref}}{C_F} = \frac{V_{DC}}{C_F},$$

with the following solution:



**Figure 4.16: Simulated line-line voltage at motor terminal for  $C_{F\_Y} = 24.6$  nF (a) and  $C_{F\_Y} = 48$  nF (b)**

$$v_{\text{ref}} = V_{\text{DC}} - K \cdot e^{\frac{-t}{(R_F + Z_{\text{Cab\_CM}})C_F}} \quad \text{Eq. 4.20}$$

The boundary conditions need to be defined to determine the constant  $K$ : at  $t = 0$ , the filter capacitor is discharged ( $V_{C\_F} = 0$ ) and the cable is seeing only the resistive part of the filter. The reflected voltage can be expressed only as a function of incident voltage:

$$v_{\text{ref}} = v_{\text{in}} \cdot K_L = v_{\text{in}} \cdot \frac{R_F - Z_{\text{Cab\_CM}}}{R_F + Z_{\text{Cab\_CM}}} \quad \text{Eq. 4.21}$$

Inserting Eq. 4.21 in Eq. 4.20, the constant  $K$  is obtained at  $t = 0$ :

$$K = V_{\text{DC}} \cdot \frac{2 \cdot Z_{\text{Cab\_CM}}}{R_F + Z_{\text{Cab\_CM}}},$$

and, finally, using Eq. 4.20 in Eq. 4.16, the expression for  $v_F$  is found :

$$v_F = v_{\text{in}} + v_{\text{ref}} = 2 \cdot V_{\text{DC}} - V_{\text{DC}} \cdot \frac{2 \cdot Z_{\text{Cab\_CM}}}{R_F + Z_{\text{Cab\_CM}}} \cdot e^{\frac{-t}{(R_F + Z_{\text{Cab\_CM}})C_F}} \quad \text{Eq. 4.22}$$

First, the filter resistance is set equal to the cable impedance to damp the voltage wave reflections. Considering the 34 m long LAPP cable, the following expression is obtained:  $R_F = Z_{\text{Cab\_CM}} = 35 \Omega$ .

The second step is to set the desired voltage overshoot. Due to the presence of the capacitances, there is still some oscillation because the complexity of the system increases. For example, at time  $t = 2t_p$  the desired voltage overshoot is 20%. Replacing  $v_F = 1.2 \cdot V_{\text{DC}}$  in Eq. 4.22, the capacitance  $C_F$  can be determined as follows:

$$1.2 \cdot V_{\text{DC}} = 2 \cdot V_{\text{DC}} - V_{\text{DC}} \cdot \frac{2 \cdot Z_{\text{Cab\_CM}}}{R_F + Z_{\text{Cab\_CM}}} \cdot e^{\frac{-t}{(R_F + Z_{\text{Cab\_CM}})C_F}} \Rightarrow 0.8 = e^{\frac{-t}{(R_F + Z_{\text{Cab\_CM}})C_F}}$$

$$\Rightarrow C_F = \frac{-2 \cdot t_p}{2 \cdot Z_{\text{Cab\_CM}} \cdot \ln(0.8)} \quad \text{Eq. 4.23}$$

Using the known values for  $t_p$  and  $Z_{\text{Cab\_CM}}$  (per-phase parameters of the 34 m long LAPP cable from Table 7.3), the filter capacitance is found:  $C_F = 24.6$  nF. Using these values for filter parameters, the results from Figure 4.16 (a) are obtained from simulations.



In Figure 4.16 (b) the simulation results for a larger capacitance value are shown. It can be noticed that the voltage overshoot is reduced, but at the same time, filter losses increase.

Finally, the design of the RC terminators represents a trade-off between overvoltage and losses. The characteristic curves, shown in Figure 4.15 (b) are obtained by varying the filter parameters. The solid lines represent the voltage overshoot (left Y axes) and dashed lines stand for losses (right Y axes). On the X-axes the filter capacitance  $C_F$  was varied and the three sets are depicted for three filter resistance:  $Z_{Cab\_CM} / 2$ ,  $Z_{Cab\_CM}$  and  $2Z_{Cab\_CM}$ . From these characteristics, possible filter implementations (parameter values) may be chosen depending on the desired compromise voltage overshoot vs. losses. For example, two pairs of filter parameters can be directly determined for two operation points: 20%  $\rightarrow$  60W and 40%  $\rightarrow$  40W, see Figure 4.15 (b). However, very good results, regarding the overvoltage at motor terminals, are obtained when  $R_F = Z_{Cab\_CM}$  is chosen.

### 4.3.3 RC-Diode clamp filters

A third type of passive cable terminator, investigated here, is based on the voltage clamping, using a rectifier bridge and power Zener diodes. This filter topology was detailed in [61] and is drawn in Figure 4.17 (a). Using the diode bridge, the line-line voltages from the cable are rectified and the half DC-link voltages are reproduced over both upper and lower  $C_F$  capacitances. The Zener diodes are used in parallel with these capacitances to clamp the voltage increase at motor terminals over a certain limit. During the voltage clamping, additional resistances are used to limit the current peaks, thus reducing the losses in the Zener diodes and protecting them.

Compared with the RC-filter topology, where only the resistive losses were accounted, due to much smaller capacitor losses, additional losses will be generated by the rectifier and Zener diodes, which cannot be neglected anymore. Therefore, the ideal models for the rectifier and Zener diodes must be replaced with real models, taking into consideration e.g. the voltage drop during conduction.

First, the rectifier diodes of the filter must have different properties than the common ones, as the clamped voltage has a much higher frequency than the power grid voltage. Moreover, they need to support high voltages and allow short currents with high amplitudes (depending on the filter parameters  $R_F$  and  $C_F$ ). Thus, an ultra-fast diode was chosen for the experimental setup with the following properties: 1200V breakdown voltage and 40A forward surge current. For losses estimations only the static characteristic (conduction losses) of the diode will be considered (see Figure 4.18 (a) depicted from data sheet [62]), as the switching losses are assumed to be negligible for this diode types.

Second, the ideal Zener diode is replaced also with a static model shown in Figure 4.18 (b), which consists of: a constant voltage source  $U_Z$ , representing the Zener threshold voltage; a resistance  $R_Z$ , which stands for the slope of the reverse current characteristic  $U_Z = f(I_Z)$ ; an auxiliary ideal diode  $D_Z$  used to allow the Zener current  $I_Z$  to flow only when

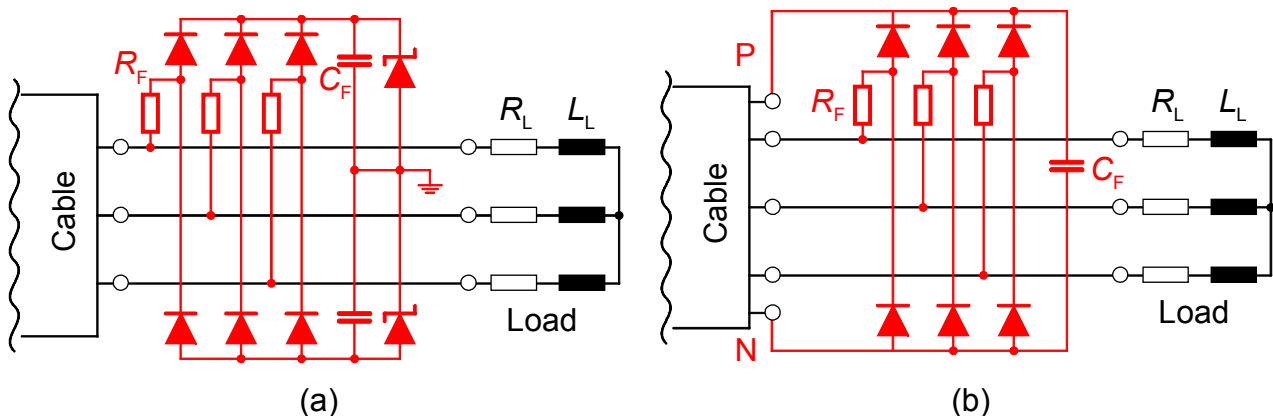


Figure 4.17: RC-Diode clamp filter topology with Zener diodes (a) and DC-link feedback (b)



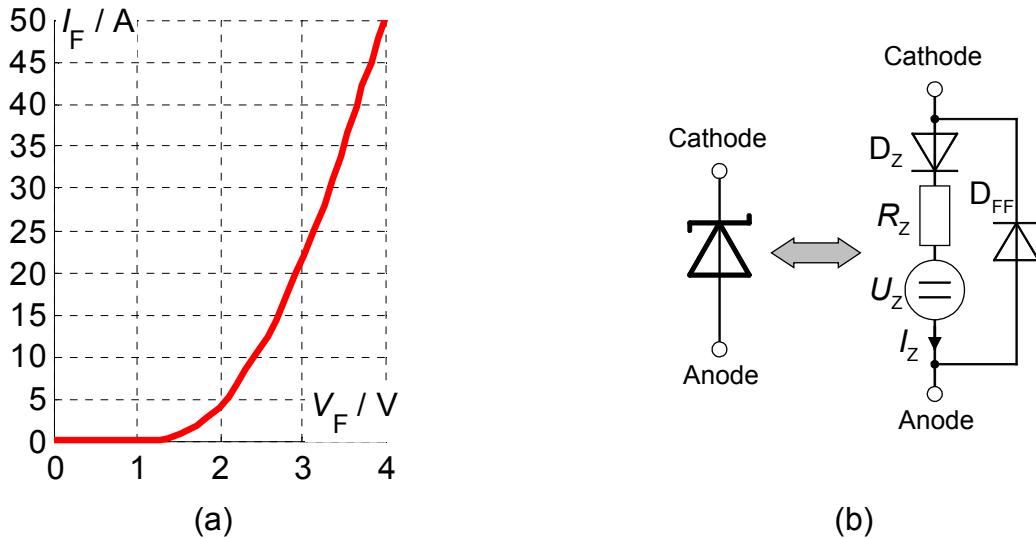


Figure 4.18: Rectifier diode charact. (a) and Static Zener diode model (b)

the threshold voltage  $U_Z$  is exceeded. In parallel, the diode  $D_{FF}$  may be used to model the forward conduction but, due to the fact that the Zener diodes are used here only to clamp the capacitor voltage, this diode may be neglected. Because the reverse current slope is very steep for Zener diodes, an external resistance ( $R_Z$  in this case) is usually used to limit  $I_Z$  and protect the device. The Zener diode with highest breakdown voltage available has  $U_Z = 200$  V and allows  $I_Z = 200$  mA maximum, [63]. This current limitation leads further to an unpractical increase of the necessary number of Zener diodes.

An equivalent circuit is proposed in [61] to emulate the power Zener diode and clamp the excess voltage across  $C_F$ . For simplification, the static model from Figure 4.18 (b) was used in simulation, whereas  $R_Z$  was chosen  $1\ \Omega$  to obtain reasonable  $I_Z$  values for an hypothetical power Zener diode. If  $R_Z$  is increased to limit  $I_Z$ , the Zener losses increase.

The total losses are presented in Figure 4.19 (a) when only one filter parameter is varied, namely resistance  $R_F$ . It can be noticed that the Zener diode losses are dominant and strongly increasing for lower  $R_F$  values. The losses in  $R_F$  are relative low compared to the ones from the Zener diodes and show a slightly decreasing trend with decrease of  $R_F$ . The smallest losses belong to the clamping diodes. In fact, these losses are very small

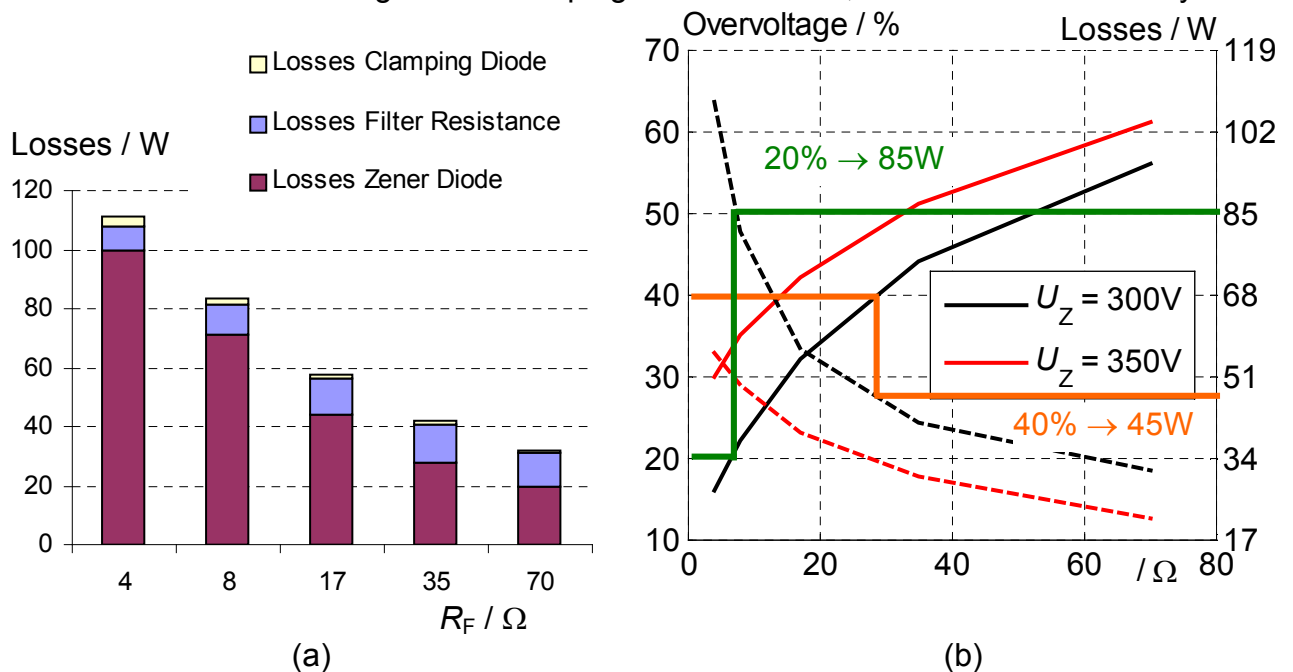
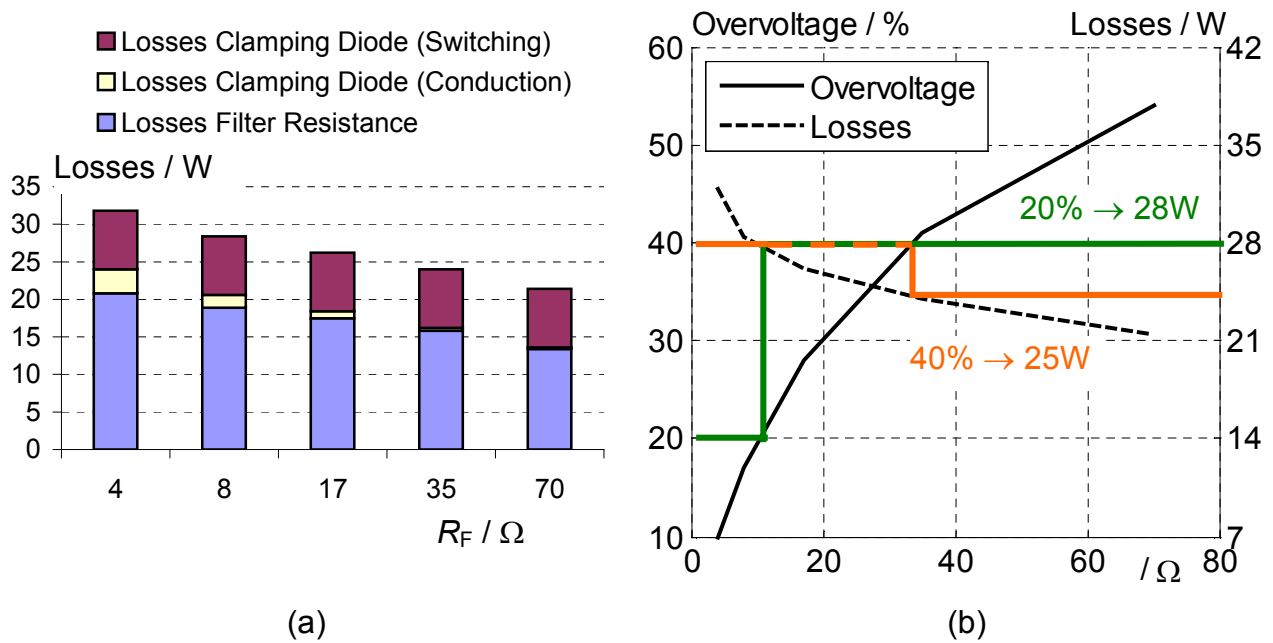


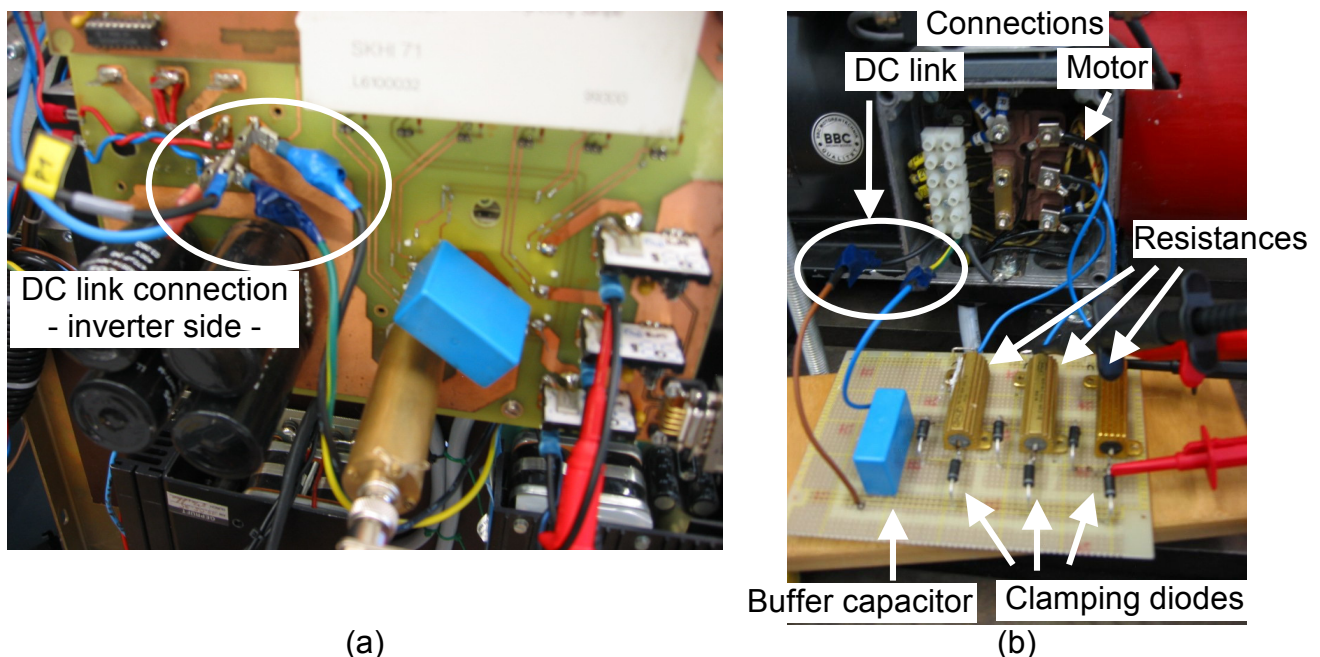
Figure 4.19: Losses distribution (a) and overvoltage/losses variation for RC-D clamp with Zener D (b)



**Figure 4.20: Losses distribution (a) and overvoltage/losses variation for RC-D clamp with DC link (b)** compared to those of the Zener diodes and therefore they are represented in Figure 4.19 (a) increased by a factor 5. It will be shown later that the switching losses of the clamp-diode are in reality not negligible. However, they play a rather minor role in this case.

Figure 4.19 (b) shows the variation of the voltage overshoot (solid line; in %) and total losses (dashed line; in Watt) depending on the filter resistance  $R_F$  and voltage level of the Zener diode. A similar trend as in the case of RC terminator is observed when  $R_F$  is decreased, i.e. the overvoltage decreases but the losses increase. A variation of  $C_F$  has a minor influence on both overvoltage and losses. Another important factor in the filter design is the choice of the Zener voltage level. Higher voltage levels lead to lower losses but increased overvoltage. Finally, this characteristic may be used as a design chart in a similar way like the characteristic for the RC filter: the filter parameters and losses are obtained directly for 20% and 40% overvoltage, see Figure 4.19 (b).

Due to the high losses in the Zener diode, especially when low overvoltage ratios are needed, a different RC-Diode clamp terminator topology was analyzed and implemented.



**Figure 4.21: DC-link connection on inverter (a) and prototype (b) of RC-Diode clamp filter**

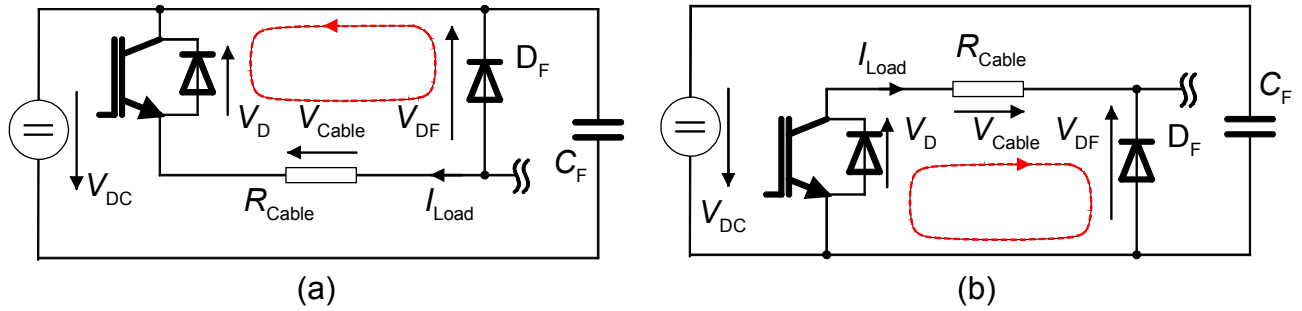


Figure 4.22: Conduction mechanism of the clamp diode from the filter for the positive (a) and negative (b) direction of the load current

Thus, the Zener diodes are removed and the upper and lower potentials of the diode bridge are connected back to the positive and negative busses of the DC-link by using two unused conductors of the same cable, e.g. the 4<sup>th</sup> and PE conductors from the 5-conductor LAPP cable, as shown in Figure 4.17 (b). A buffer capacitor is connected at the output of the diode bridge to reduce the voltage oscillations due to the cable length.

The principle is same as in the previous case, i.e. the voltage reflections are clamped using the diode bridge. A part of the energy, taken from reflections, is dissipated on the damping resistors but most of it will be fed back to the DC link, thus increasing the filter efficiency. A prototype of this filter type was constructed and tested. Figure 4.21 (a) shows the DC-link connection at the inverter, using two additional conductors from the LAPP cable. The prototype is pictured in Figure 4.21 (b). All the elements are visible on the test board together with the connections to the motor.

The estimated losses, represented in Figure 4.20 (a) (from simulations), are considerably lower than in the previous filter topology with Zener diodes. However, the clamping-diode losses can be divided into two categories:

- **conduction losses** – This filter topology shows increased conduction losses of the diodes, in both simulation and measurement, when the load current is increased. The voltage drop on the cable, due to the load current magnitude and direction, determines a positive bias voltage and, therefore, the corresponding clamp diode will conduct, like in Figure 4.22 shown for both directions of the load current. The filter resistance  $R_F$  limits the resulting current. The lower the  $R_F$  values are, the higher the current levels through the clamping diodes are, resulting in higher conduction losses, see Figure 4.20 (a).

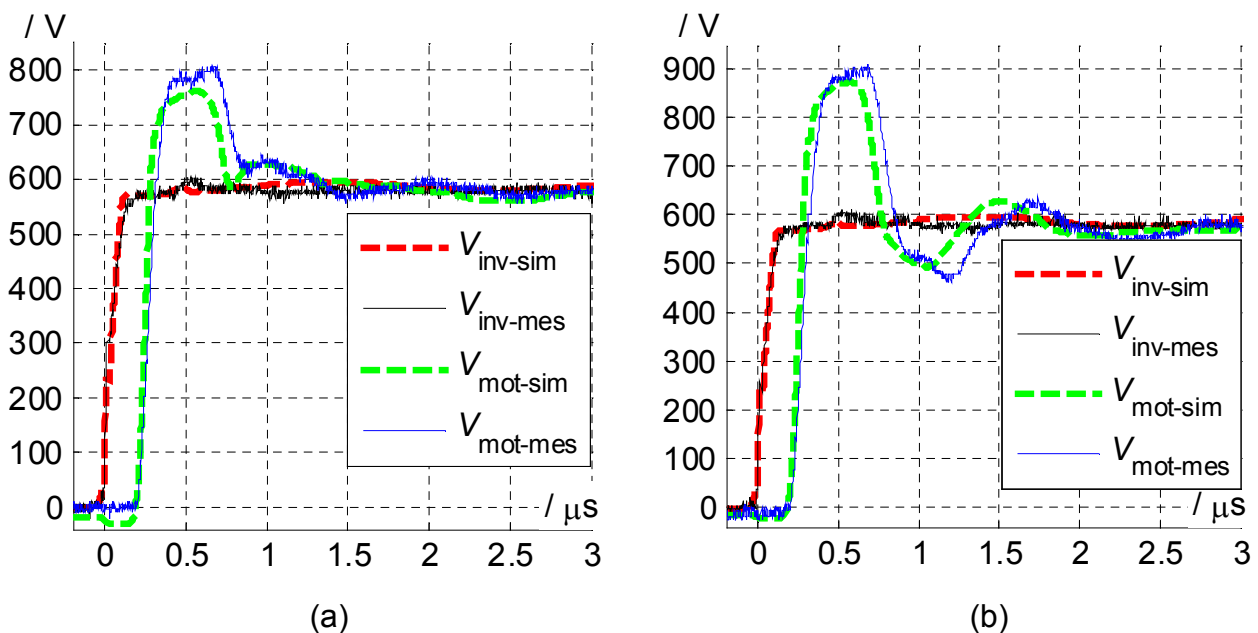


Figure 4.23: Measurements vs. simulations for  $R_F = 18 \Omega$  (a) and  $R_F = 50 \Omega$  (b)

- **switching losses** – being neglected in previous case, they become important due to the low total losses. Because there is no information in data sheet about the recovery energy [62], the switching losses are difficult to estimate. Therefore, they are first measured and then considered in simulations only for the worst case. Thus, constant additional losses of app. 7.4 W are represented in Figure 4.20 (a).

The overvoltage and total losses variation with  $R_F$  is shown in Figure 4.20 (b). For both RC-diode clamp topologies, an overvoltage less than 20% is obtained for small values of the filter resistance ( $R_F < Z_C/2$ ), when compared to the RC terminator topology. Here, the optimal value was  $R_F = Z_C$ , see Figure 4.15 (b). For a 20% and 40% voltage overshoot, the losses and filter resistance are determined directly from the plotted characteristic, as shown in Figure 4.20 (b).

Finally, the simulations and measurements are shown in Figure 4.23 for the RC-diode clamp filter topology with DC-link feedback, using two different values for  $R_F$ : 18  $\Omega$  and 50  $\Omega$ . As expected, a smaller voltage overshoot is observed for a smaller resistance value. Also, a good agreement between simulations and measurements is obtained, thanks to the accurate simulation models.

## 4.4 Use of inverter output filters

The operation principle for this type of filters is: having additional line inductors, the filters at the inverter output reduce the voltage overshoot at the motor terminals by decreasing the voltage slope at the inverter output. This brings other advantages, like smaller displacement currents in the cable and motor, but higher losses occur due to the additional inductors crossed by the full load current (resistive and core losses). Further, several filter topologies are analyzed together with their design algorithms. Because the losses estimation is much more difficult for inductors due to the many unknown variables, like conductor diameter or core properties, the losses for this type of filters will not be considered further but only the effect on overvoltage and  $R_F$  losses.

### 4.4.1 RL filter

The simplest inverter output filter can be realized with line chokes at the inverter output, see Figure 4.24 (a). Because the inductors alone introduce large oscillations, parallel resistors are used to damp these oscillations. Such filter topology was introduced in [37] together with the design method. Filter design starts with the simplified equivalent circuit of the cable from Figure 4.24 (b), where the inductor and resistor of the filter are added. The transfer function of the entire circuit from Figure 4.24 (b) can be expressed as follows:

$$G(s) = \frac{V_{\text{mot}}}{V_{\text{inv}}} = \frac{(s \cdot L_F + R_F) \cdot \frac{1}{L_{\text{Tot\_DM}} C_{\text{Tot\_DM}} L_F}}{s^3 + s^2 \left( \frac{1}{L_{\text{Tot\_DM}}} + \frac{1}{L_F} \right) R_F + s \left( \frac{1}{L_{\text{Tot\_DM}} C_{\text{Tot\_DM}}} \right) + \frac{R_F}{L_{\text{Tot\_DM}} C_{\text{Tot\_DM}} L_F}}, \quad \text{Eq. 4.24}$$

which has the following characteristic equation:

$$s^3 + s^2 \left( \frac{1}{L_{\text{Tot\_DM}}} + \frac{1}{L_F} \right) R_F + s \left( \frac{1}{L_{\text{Tot\_DM}} C_{\text{Tot\_DM}}} \right) + \frac{R_F}{L_{\text{Tot\_DM}} C_{\text{Tot\_DM}} L_F} = 0. \quad \text{Eq. 4.25}$$

The nonoscillatory condition for Eq. 4.24 is given by the expression  $D \geq 0$ , where  $D$  represents the discriminant of Eq. 4.25. Following relation is obtained for  $D = 0$ :

$$\frac{R_F^2}{L_{\text{Tot\_DM}} / C_{\text{Tot\_DM}}} = \frac{n^2}{8 \cdot (n+1)^2} \cdot [n^2 + 20 \cdot n - 8 \pm (n-8) \sqrt{n \cdot (n-8)}] = A \pm B \sqrt{k}, \quad \text{Eq. 4.26}$$

$$\text{with } n = L_F / L_{\text{Tot\_DM}}, \quad A = \frac{n^2}{8(n+1)^2} (n^2 + 20n - 8) \quad \text{and} \quad B \sqrt{k} = \frac{n^2}{8(n+1)^2} (n-8) \sqrt{n(n-8)}.$$

Finally, the nonoscillatory conditions are found:

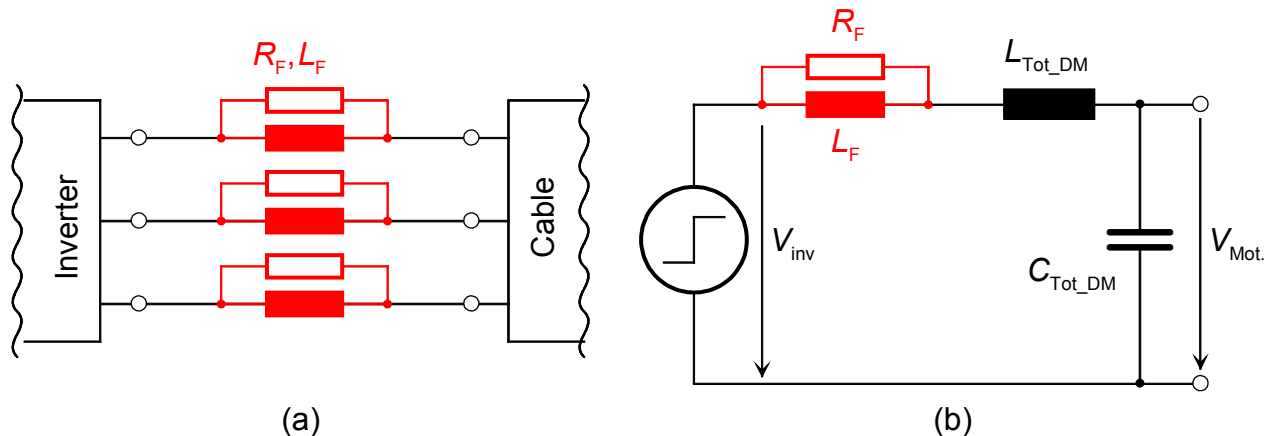
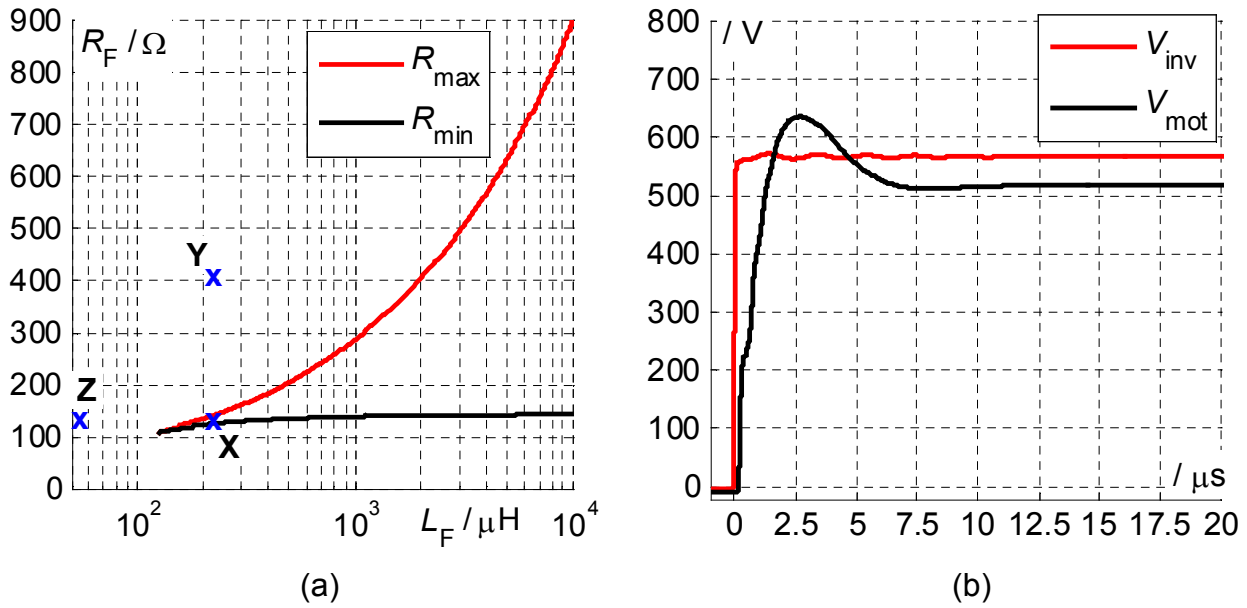


Figure 4.24: RL filter topology (a) and equivalent circuit for filter design (b)

Figure 4.25: Parameter characteristic (a); simulated  $V_{\text{inv}}$  and  $V_{\text{mot}}$  for point X (b)

$$a) L_F \geq 8 \cdot L_{\text{Tot\_DM}},$$

$$b) (A - B\sqrt{k}) < \frac{R_F^2}{L_{\text{Tot\_DM}} / C_{\text{Tot\_DM}}} < (A + B\sqrt{k}).$$

Eq. 4.27

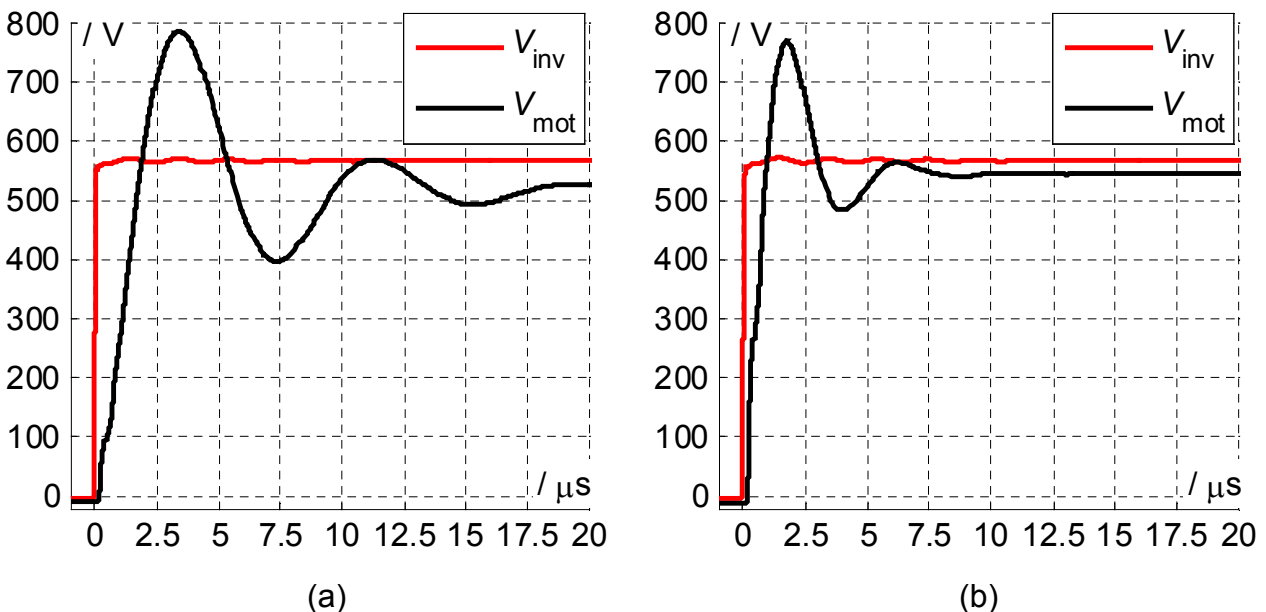
Inserting the values for the LAPP Cable,  $L_{\text{Tot\_DM}} = L'_{\text{DM}} \cdot l = 15.64 \mu H$  (see Table 7.3) and  $C_{\text{Tot\_DM}} = C'_{\text{DM}} \cdot l = 3.128 \text{ nF}$  (see Table 7.3), the parameter values of the filter are obtained:  $L_F = 8 \cdot L_{\text{Tot\_DM}} \approx 125 \mu H$ ; from Eq. 4.26  $\Rightarrow R_F = 108 \Omega$ .

Also, from Eq. 4.26, the minimal and maximal value for  $R_F$  may be derived:

$$R_{F\_min} = \sqrt{\frac{L_{\text{Tot\_DM}}}{C_{\text{Tot\_DM}}}} \cdot \sqrt{\frac{n^2}{8 \cdot (n+1)^2} \cdot [n^2 + 20 \cdot n - 8 - (n-8)\sqrt{n \cdot (n-8)}]},$$

$$R_{F\_max} = \sqrt{\frac{L_{\text{Tot\_DM}}}{C_{\text{Tot\_DM}}}} \cdot \sqrt{\frac{n^2}{8 \cdot (n+1)^2} \cdot [n^2 + 20 \cdot n - 8 + (n-8)\sqrt{n \cdot (n-8)}]}.$$

Eq. 4.28

Figure 4.26: Simulated  $V_{\text{inv}}$  and  $V_{\text{mot}}$  for point of operation Y (a) and Z (b)



Computing the expressions from Eq. 4.27 and Eq. 4.28 in Matlab, the characteristic of the filter parameters is plotted in Figure 4.25 (a). The area between  $R_{F\_min}$  and  $R_{F\_max}$ , also called nonoscillatory region, is the region in which the parameters fulfill the nonoscillatory condition of the transfer function (Eq. 4.24).

Further, three points of operation, i.e. three pairs of parameter values, are chosen to simulate the filter. In Figure 4.25 (b), the simulated inverter output and motor input voltages are plotted for point **X** ( $L_F = 200 \mu\text{H}$ ,  $R_F = 120 \Omega$ ), which is situated inside the nonoscillatory region. A voltage overshoot of app. 23%, with respect to the steady-state voltage at the motor terminals, is observed. It must be mentioned that due to the relative high inductor value, the voltage at the motor terminal is smaller than the DC-link level, as the voltage drop along the line chokes is high. This leads further to high losses especially at high load currents and high inductor values. The same voltages are plotted in Figure 4.26 at other points of operation from outside the nonoscillatory region, namely point **Y** ( $L_F = 200 \mu\text{H}$ ,  $R_F = 400 \Omega$ ) in Figure 4.26 (a) and point **Z** ( $L_F = 55 \mu\text{H}$ ,  $R_F = 120 \Omega$ ) in Figure 4.26 (b). The increase of resistance value  $R_F$  leads to an increase of the filter time constant (lower  $dV/dt$ ), but the damping constant of the filter is altered and the overvoltage increases up to 50%. However, the reduction of inductor value  $L_F$  decreases both the time (higher  $dV/dt$ ) and the damping constants, leading to 41% voltage overshoot. A lower inductor value yields lower voltage drop at the filter (26 V compared to 53 V from point **X** in the considered example) and lower losses.

#### 4.4.2 RLC filter

An improvement of the RL inverter output filter represents the RLC filter where the addition of new reactive elements, i.e. capacitors, allows a better efficiency for the line chokes. This filter topology is frequently used in the industry to suppress the voltage overshoot at the motor terminals. It consists of line chokes and series connected resistances and capacitances; see Figure 4.27 (a) [31].

Very important to know for the design of this filter topology is the wave oscillation period of the cable. For exemplification, the 34 m long LAPP cable will be further considered. From section 7.1.1, an oscillation period  $T_{osc} = 4t_p \approx 970 \text{ ns}$  can be determined, see Table 7.3. Thus, the cutoff frequency is expressed:  $f_{co} = 1/T_{osc} \approx 1.031 \text{ MHz}$ . In the next step, the filter resistance is set equal to the cable impedance, in this case  $R_F = Z_{Cab\_CM}$ . Finally, the filter inductance and capacitance are calculated from the transfer function of the filter:

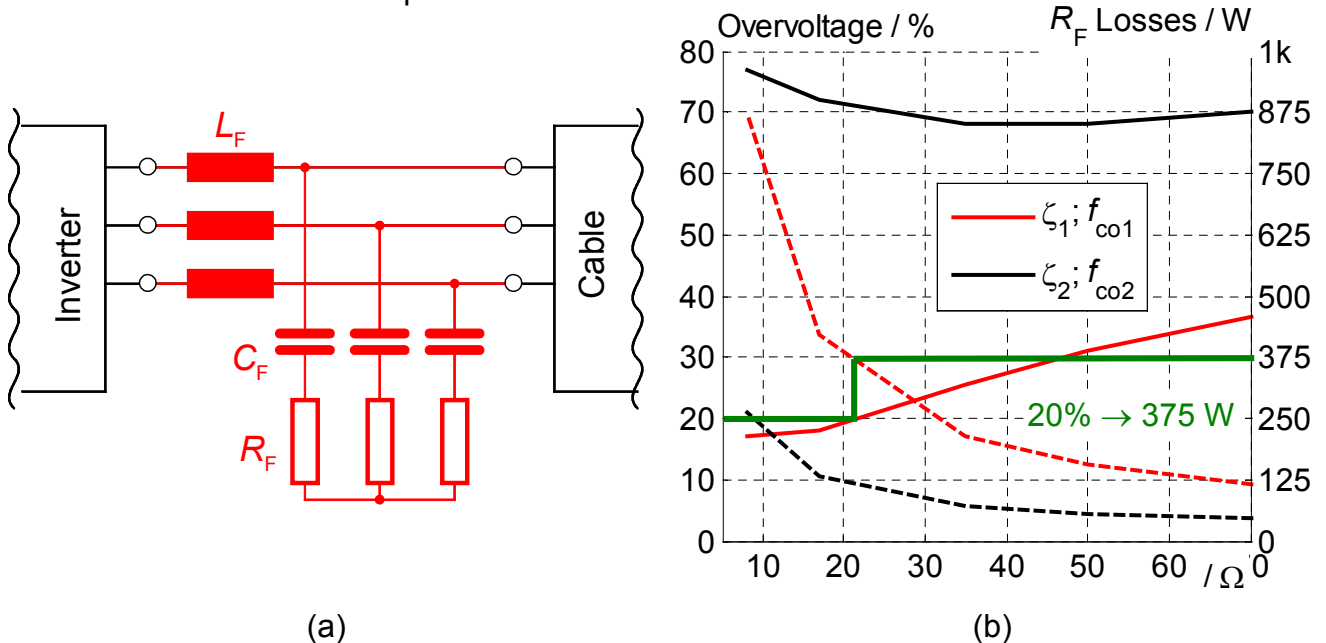


Figure 4.27: RLC filter topology (a); overvoltage and resistor losses dependency on  $R_F$ (b)

$$G(s) = \frac{V_{\text{filt\_out}}}{V_{\text{filt\_in}}} = \frac{s \cdot R_F C_F + 1}{s^2 \cdot L_F C_F + s \cdot R_F C_F + 1} = \frac{R_F / C_F \cdot (s + 1/R_F C_F)}{s^2 + s \cdot (R_F / C_F) + 1/(L_F C_F)} \quad \text{Eq. 4.29}$$

From Eq. 4.29, the main parameters of the transfer function are:

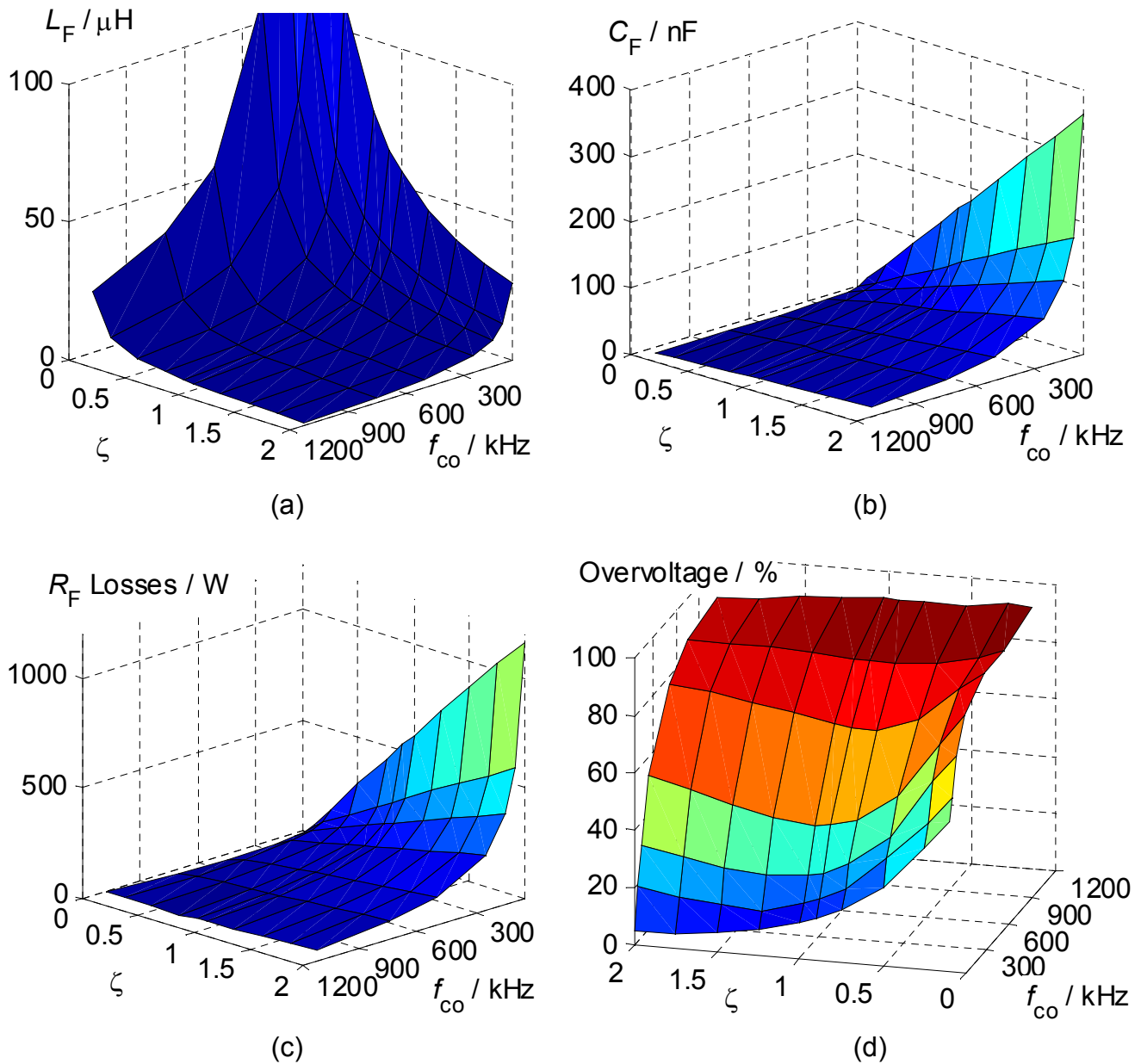
$$\omega_{\text{co}} = 2\pi \cdot f_{\text{co}} = \frac{1}{L_F \cdot C_F} - \text{the cutoff frequency expressed in sec}^{-1},$$

$$\frac{R_F}{L_F} = 2\zeta \cdot \omega_n \Rightarrow \zeta = \frac{R_F}{2} \sqrt{\frac{C_F}{L_F}} - \text{the damping of the filter.} \quad \text{Eq. 4.30}$$

Solving Eq. 4.30 for  $L_F$  and  $C_F$ , the following expressions are found:

$$C_F = \frac{2\zeta}{R_F \cdot \omega_{\text{co}}}; \quad L_F = \frac{1}{C_F \cdot \omega_{\text{co}}^2}.$$

Depending on the chosen cutoff frequency, the RLC inverter filters are classified in two categories:



**Figure 4.28:** Variation of  $L_F$  (a) and  $C_F$  (b) with damping  $\zeta$  and cutoff frequency  $f_{\text{co}}$ ; Variation of  $R_F$  losses (c) and overvoltage (d) with damping  $\zeta$  and cutoff frequency  $f_{\text{co}}$ .



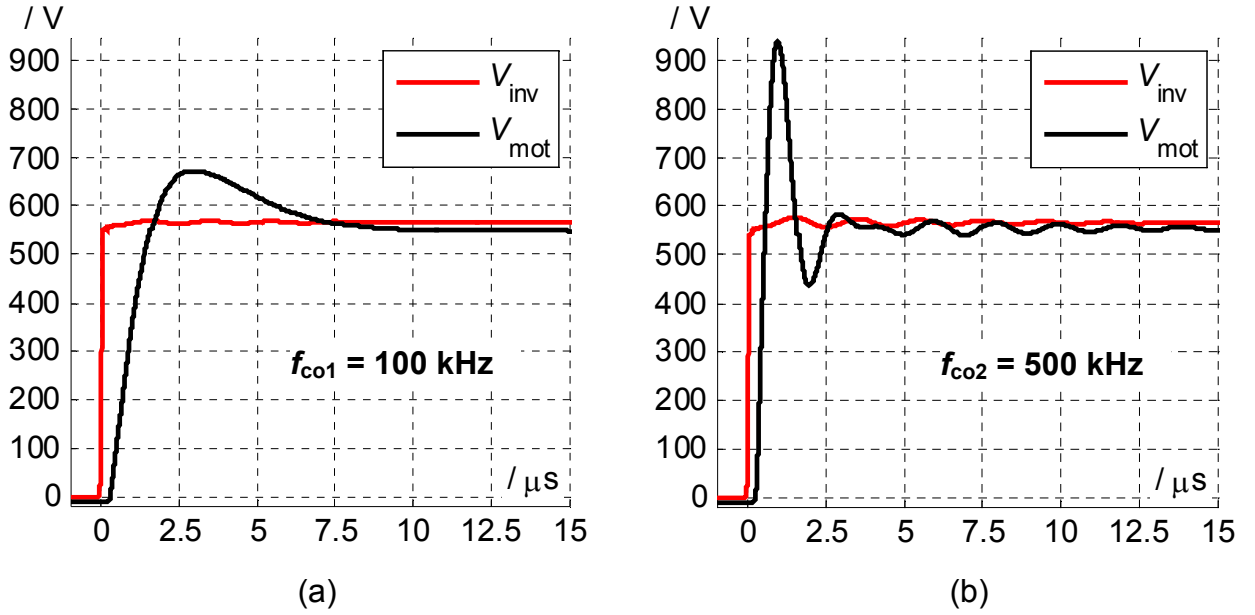


Figure 4.29: Simulated  $V_{inv}$  and  $V_{mot}$  for parameter pairs  $(\zeta_1; f_{co1})$  (a) and  $(\zeta_2; f_{co2})$  (b)

- **dV/dt filters**, where the cutoff frequency is set between the switching frequency and the oscillation frequency of the voltage wave on the cable. As effect, the voltage rise time is reduced but the voltage maintains the pulsed shape at the filter output;

- **Sine-Wave filters**, whose cutoff frequency is chosen between the fundamental and the switching frequency. In this case the voltage is filtered from rectangular blocks to a sinusoidal shape with the frequency equal to the fundamental frequency of the motor. Thus, the filter has more losses than the previous type (better filtering), but the motor losses are reduced considerably as no longer pulsed voltages are applied to it.

A dV/dt inverter filter will be further analyzed in detail for exemplification, whose cutoff frequency is chosen between the switching and the oscillation frequency of the wave on the cable. Because there is a large degree of freedom in choosing the cutoff frequency  $f_{co}$  and the damping constant  $\zeta$ , they have been varied in a wide range:  $f_{co}$  from 50 kHz to 1.125 MHz and  $\zeta$  from 0.1 to 2 ( $\zeta < 1 \rightarrow$  underdamped system;  $\zeta > 1 \rightarrow$  overdamped system) [31]. Finally, the filter parameters are calculated. The  $L_F$  and  $C_F$  dependency on  $f_{co}$  and  $\zeta$  is represented in Figure 4.28 (a) and (b), respectively, for a fixed resistance value ( $R_F = 35 \Omega$  for the LAPP cable). As expected, a lower cutoff frequency determines higher values for both  $L_F$  and  $C_F$ . On the contrary, the damping constant of the filter leads to an opposite variation, i.e. the inductor values increase while decreasing  $\zeta$ ; the capacitor values decrease for the same trend of  $\zeta$ . As already mentioned, the additional capacitance  $C_F$  for the RLC inverter filter allows, for same overvoltage ratio, a considerably reduction of the inductor size with respect to the RL filter, e.g.  $L_{F\_RLC} \approx 15 \mu H$  and  $L_{F\_RL} \approx 200 \mu H$  for app. 24% voltage overshoot.

Inserting the calculated values in the simulation model, the overvoltage characteristic from Figure 4.28 (d) is obtained. It is obvious that a better damping of the oscillations on the cable is obtained for a smaller cutoff frequency. However, both high and low values of  $\zeta$  change the filter properties (higher overvoltage ratio). Thus, the optimal overvoltage reduction is obtained around the value  $\zeta = 1$ . Additionally, the resistance losses  $P_{R\_F}$  of the filter were computed from simulations and are presented in Figure 4.28 (c). Although they do not reflect the total losses,  $P_{R\_F}$  illustrates the strong increase of the resistance losses for low values of  $f_{co}$ . Again it is clear that a better damping of the oscillations occurs only with higher losses, i.e. the lower cutoff frequency and higher  $\zeta$  lead automatically to higher  $P_{R\_F}$  losses. Based on these characteristics, a compromise between the overvoltage attenuation and the filter losses has to be chosen when designing this filter. To analyze the

effect of the filter resistance  $R_F$ , the characteristics “overvoltage ratio (solid line) and  $P_{R_F}$  (dashed line) vs.  $R_F$ ” are plotted in Figure 4.27 (b) for two pairs of filter properties:

- ( $\zeta_1 = 1$ ;  $f_{co1} = 100$  kHz) – a good reduction of the voltage overshoot is obtained due to the lower cutoff frequency. As the  $R_F$  value decreases, the overvoltage ratio decreases, too, while the losses increase;
- ( $\zeta_2 = 1$ ;  $f_{co2} = 500$  kHz) – a poor reduction of the voltage overshoot is obtained due to the higher cutoff frequency. Decreasing the  $R_F$  values determine higher losses but the overvoltage ratio presents a minimum at  $R_F = Z_{Cab\_CM}$ .

From Figure 4.27 (b) it can be concluded that,  $R_F = Z_{Cab\_CM}$  represents an optimal choice which leads to a minimal overvoltage/ $P_{R_F}$  ratio. For the 20% desired overvoltage, the resistive losses are relative high (375 W) compared to the other inverter-output filters. However, these losses depend strongly on the filter design, so a compromise must be chosen between the filter losses and the effect at the inverter output. The characteristic from Figure 4.27 (b) offers a preliminary design rule.

Finally, the simulated voltage at the inverter output and motor terminals are plotted in Figure 4.29 for two sets of parameters:

- ( $R_F = 35 \Omega$ ;  $\zeta_1 = 0.9$ ;  $f_{co1} = 100$  kHz) in Figure 4.29 (a) – due to the lower bandwidth of the filter, a small voltage slope at the motor terminal is observed ( $\approx 432$  V/ $\mu$ s), which leads to a lower voltage overshoot (20%);
- ( $R_F = 35 \Omega$ ;  $\zeta_2 = 0.9$ ;  $f_{co2} = 500$  kHz) in Figure 4.29 (b) – opposite to the previous case, the higher cutoff frequency determines a higher voltage slope at the motor terminals ( $\approx 1.97$  kV/ $\mu$ s), leading to 67% voltage overshoot.

#### 4.4.3 RL-Diode clamp filter

The last filter topology investigated in this section is the RL-diode clamp filter. Having the oscillations reduced in the previous case by a combination of three passive elements ( $L_F$ ,  $C_F$  and  $R_F$ ), the large oscillations due to additional line chokes are clamped in this case using a diode bridge rectifier connected to the DC link, see Figure 4.30. This filter topology was presented in [61] together with the RC-diode clamp. In fact, the topology reassembles a lot with that of the RC-diode clamp terminator, except of the additional line chokes. The diode bridge rectifier is connecting all the three phases to the positive and negative DC-link bus bars. The additional resistances are limiting the current through these diodes and reduce the losses.

The principle of operation is: the line chokes are used to reduce the voltage gradient at the inverter output; because the chokes alone cause high voltage overshoot at the filter output, the additional diodes clamp this voltage to the DC-link value by having the upper and lower side of the rectifier bridge connected to the DC-link positive and negative rails, respectively; thus a part of the energy is fed back to inverter.

For example, the same 34 m LAPP cable is considered between inverter and motor. As suggested in [61], the filter resistance is first set to  $R_F = Z_{Cab\_CM}$ . The filter model is similar

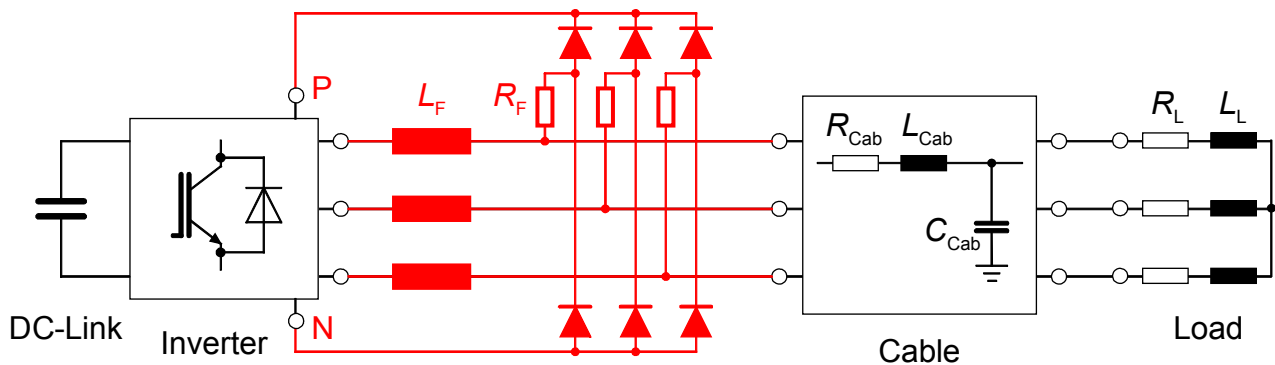


Figure 4.30: RL-diode clamp inverter output filter topology

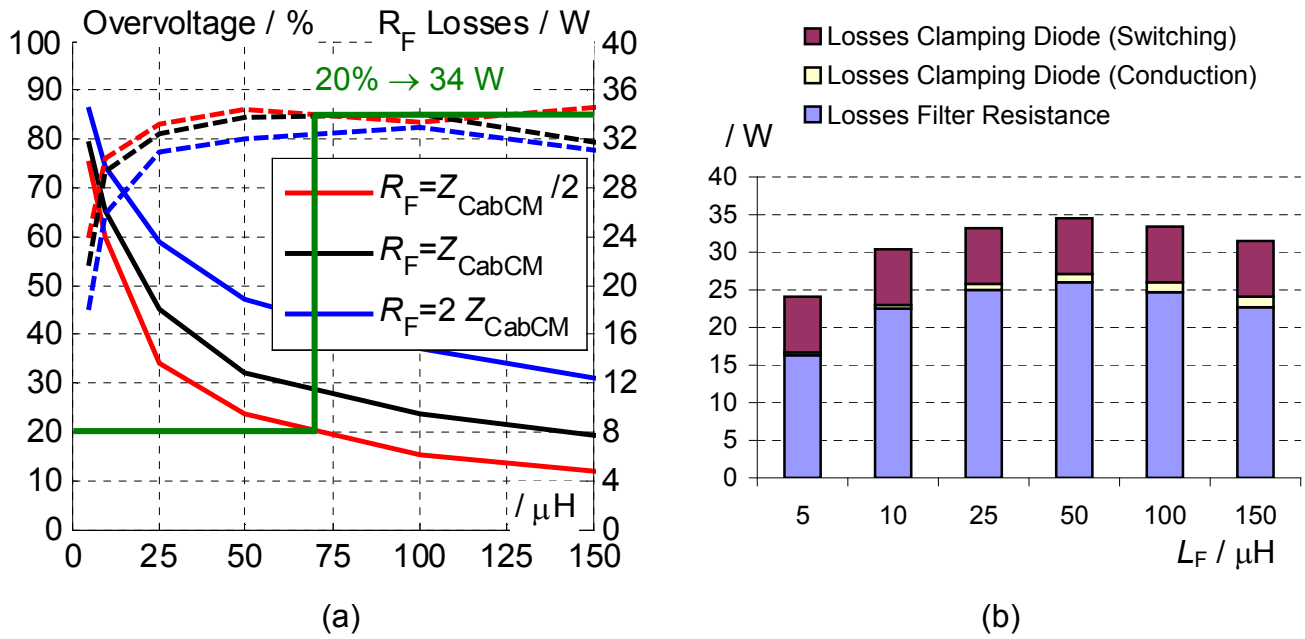


Figure 4.31: Overvoltage (solid) and  $P_{\text{RF\_D}}$  (dashed) vs.  $L_F$  and  $R_F$  (a); distributed  $P_{\text{RF\_D}}$  (b) vs.  $L_F$

to the one from section 4.3.3 with the DC-link feedback, i.e. the clamping diodes are modeled using the output characteristic  $I_F = f(V_F)$ . The inductor losses will be further neglected due to the complicate and various design. However, the resistance and diode losses ( $P_{\text{RF\_D}}$ ) will be further considered in order to get an idea of the trend.

To determine the optimal inductor value, several simulations with parameter variation were conducted. The dependency of the overvoltage and  $P_{\text{RF\_D}}$  losses on filter parameters is plotted in Figure 4.31 (a). Here it can be noticed that, similar like in the case of RC-diode clamp motor filter, the optimal  $R_F$  resistance value is  $R_F = Z_{\text{Cab\_CM}}/2$ . The RL-diode clamp inverter filter determines the lowest overvoltage at this value, while keeping the losses  $P_{\text{RF\_D}}$  at the same level.

The distribution of the losses between the resistor  $R_F$  and the clamping diode is shown in Figure 4.31 (b), when  $L_F$  is varied and  $R_F = 18 \Omega$  is fixed. As in the case of RC-diode clamp terminator, the diode conduction and switching losses are small compared to the resistor losses. Therefore, the measured switching losses (worst case app. 7.4 Watt) from

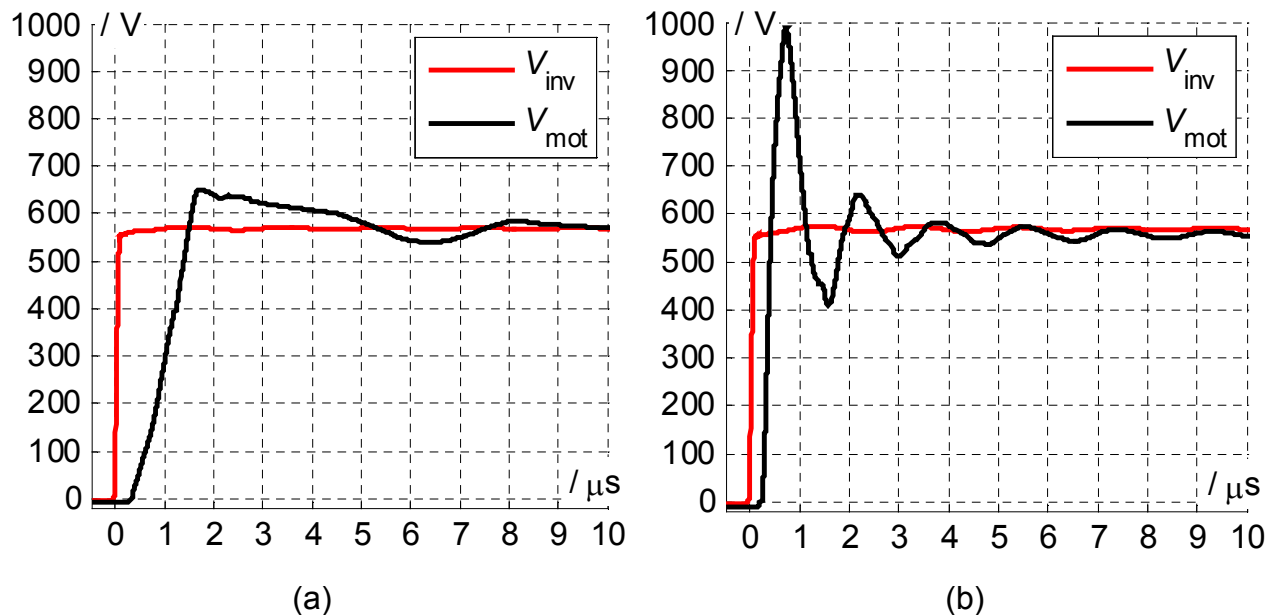


Figure 4.32: Simulated  $V_{\text{inv}}$  and  $V_{\text{mot}}$  for  $L_F = 100 \mu\text{H}$  (a) and  $L_F = 5 \mu\text{H}$  (b)

RC-diode clamp terminator will be adopted also here and added to the estimated  $P_{RF\_D}$ .

The final simulations for the two different  $L_F$  values show the principle of the RL-diode clamp filter. In Figure 4.32 (a)  $L_F$  is 100  $\mu\text{H}$ , which determines a small voltage slope. Still, the voltage tends to oscillate further as there is no capacitor for compensation. At this point, the diode limits the possible oscillations and the voltage at the motor terminals does not exceed 15% overvoltage ratio. If  $L_F$  is kept small, e.g. 5  $\mu\text{H}$ , the voltage at the motor terminals presents a high overshoot, like in Figure 4.32 (b) shown. This happens due to the small energy buffer at inverter output ( $L_F$ ) and the relative high  $R_F$  resistance for this small  $L_F$  (it limits the energy flow back to DC link). Therefore, the use of small inductors is not optimal.

To conclude, several basic filter topologies were analyzed and their parameters calculated for a wide range. Using the developed simulation models connected together in the inverter-cable-motor system, the filters are tested and the results obtained for the overvoltage/losses characteristics considering a large spectrum of parameters. Plotting the overvoltage vs. parameters and losses vs. parameters characteristics, an optimal pair of parameters is obtained, even when no specific filter equations can be derived. This entire process takes place off-line, i.e. using only simulations and saving a lot of time for hardware testing.

Starting from these basic filter topologies, more complex filter may be designed with better efficiency. Also, active components can be added, which lead to the active filter topologies. A thorough overview of the overvoltage reduction methods studied here is offered in chapter 6.

## 5 Quasi resonant DC-link converter in electric drives with long cables

### Preamble

The research work concerning this chapter was done in a close cooperation between Mrs. Jayalakshmi Kedarisetti and me. Two common publications [68] and [72] contain a part of this work. In detail, the work of Mrs. Kedarisetti comprises:

- Deriving the analytical state equations for the operating modes of the two Quasi-resonant (QR) DC-link converters investigated here (see section 5.1.1)
- Development of the method and the program for calculation of the trip currents resulting in characteristics from Figure 5.7 (see section 5.1.2)
- Design, realization and commissioning of the resonant converter (including the resonant inductor design – section 5.2.2) and the FPGA-based control unit (see Figure 5.16 from 5.2.3)
- Development of the FPGA-firmware to control the QR DC-link converter
- Development of the special modulation schemes for the zero-voltage-vector implementation (see Figure 5.12 from section 5.1.4)
- Simulations of and measurements at the QR DC-link converter (see subchapter 5.3)
- Efficiency measurements for the QR DC-link converter and HS converter with output filter (see section 5.3.5)

Under the supervision of both Mrs. Kedarisetti and mine, the work from diploma thesis no: DA1347 [80] from our institute comprises:

- Investigation of semiconductor types for the QR DC-link operation, see sections 5.1.3 and 5.2.1
- Realization of the hardware setup (power part) for the QR DC-link converter

The research topic of Mrs. Kedarisetti merged with mine in the frame of the DFG research group FOR575, 2<sup>nd</sup> phase regarding “Motor-friendly and highly efficient electric converters”.

In order to present a complete and coherent description of the joint research work, the topics dealt with by Mrs. Kedarisetti are merged in this chapter with my work and presented briefly.

The cost of semiconductors shows a negative trend over the last years, which is more pronounced than the one for passive filter elements. Therefore, it is preferable to keep the number and size of inductors and capacitors as low as possible. This can be achieved with higher switching frequencies, but it leads automatically to higher switching losses for the hard-switched semiconductors. Two different approaches to reduce the switching losses are distinguished:

- the use of semiconductor-switches that are optimized for high switching frequencies;
- the use of resonant switching.

For the first approach intensive researches, started several years ago, delivered new semiconductor materials like Silicon Carbide (SiC), leading further to new and better switches: SiC-JFET or SiC-DMOSFET [64]. However, such semiconductor devices are presently available only at the prototype level. Research on soft-switching converters has been already conducted for many years and the results are available in literature [66]. A special category of interest, for the use in electric drives with long cables, is the quasi-resonant converter topology. Studies are already available for the low and middle power levels [67]. For this type of converters, the phase-to-phase voltage represents a segment from a sinusoidal voltage as a result of a resonant operation. Thus, the voltage slope  $dV/dt$  can be influenced directly by the resonant circuit and be reduced to a desired value. Additional to the switching loss reduction, the resonant circuit fulfils also the task of the 3-phase filter to reduce the voltage overshoot at the motor terminals.

A second task of the quasi-resonant converter, which will be detailed later, represents the reduction of the common-mode (CM) voltage, a well-known reason for EDM bearing currents [16]. This is achieved by adding additional switches to the resonant circuit in order

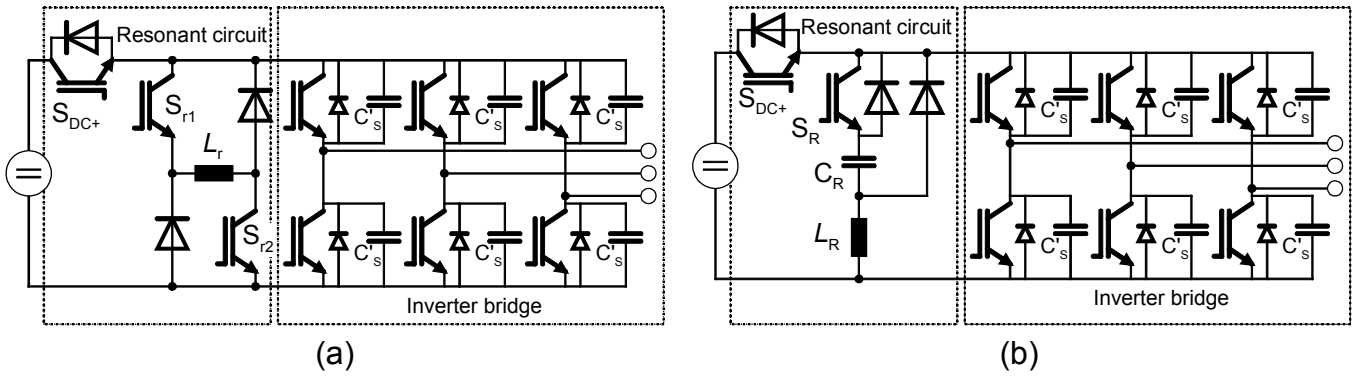


Figure 5.1: Quasi-resonant topology T1 [69] (a) and T2 [70] (b)

to separate completely the DC link from the inverter bridge [68]. Thus, the CM voltage is reduced from  $\pm V_{DC}/2$  to  $\pm V_{DC}/6$  level. In this way, the important functions of the inverter output filter are integrated in a single converter topology.

Finally, there are two application examples to test and compare: the hard-switched converter with an output filters vs. the quasi-resonant DC-link converter. Aspects like efficiency and effect on motor overvoltage must be evaluated for both applications.

Theoretical aspects, regarding different quasi-resonant converter topologies and method to optimize the functionality of such converters are discussed in subchapter 5.1. The hardware design and implementation is then presented in subchapter 5.2. Finally, the measurement results and evaluations are offered in subchapter 5.3.

## 5.1 Quasi-resonant DC-link converter topologies

The soft-switching operation of semiconductors is nowadays an alternative to the hard switching, due to the reduction of the switching losses. They are reduced considerably when one of the involved quantities (voltage or current) is set to zero, i.e. there is Zero Current Switching (ZCS) or Zero Voltage Switching (ZVS) [41]. For that, a resonant circuit, containing passive elements and active switches, generates the oscillations of the state variables (voltage or current), allowing the main switching devices to be turned on or off when one state variable is zero. Moreover, introducing the active switches to the resonant circuit, the resonant operation is initiated by the user, allowing user-defined pulse patterns, like PWM, to be implemented. Such converters are called quasi-resonant (QR) converters due to the user-defined initiation of the resonant operation. Many resonant converters topologies were developed in the literature aiming for an increased efficiency [66]. Another important aspect in the electric drives with long cables is the motor-friendly characteristic. The QR DC-link converters provide reduced voltage gradients at the inverter output during the resonant operation, as they depend now on the passive elements from the resonant circuit and no longer on the hard-switched semiconductors. By choosing the design constraints for the voltage slopes (e.g.  $dV/dt_{min}$  for a certain cable length), a safe operation margin for motors, when long cables are used, is offered.

Two quasi-resonant DC-link converter topologies from literature [67], found to deliver the best efficiency, are analyzed in this work. First, the resonant circuit from Figure 5.1 (a) is realized mainly with two passive elements ( $L_R$  and  $C'_s$ ) and three switches [69]. This topology will be called further the topology T1. The main advantage of the topology T1 is the simple control of the resonant operation, as the existence of two passive elements simplifies the circuit equations.

The second topology from [70] is shown in Figure 5.1 (b) and will be called further the topology T2. The main advantage in this case represents the reduced power dissipation in the resonant circuit because the main inductance  $L_R$  shares the energy with the additional resonant capacitor  $C_R$ . Also, fewer switches in the resonant circuit are necessary, but

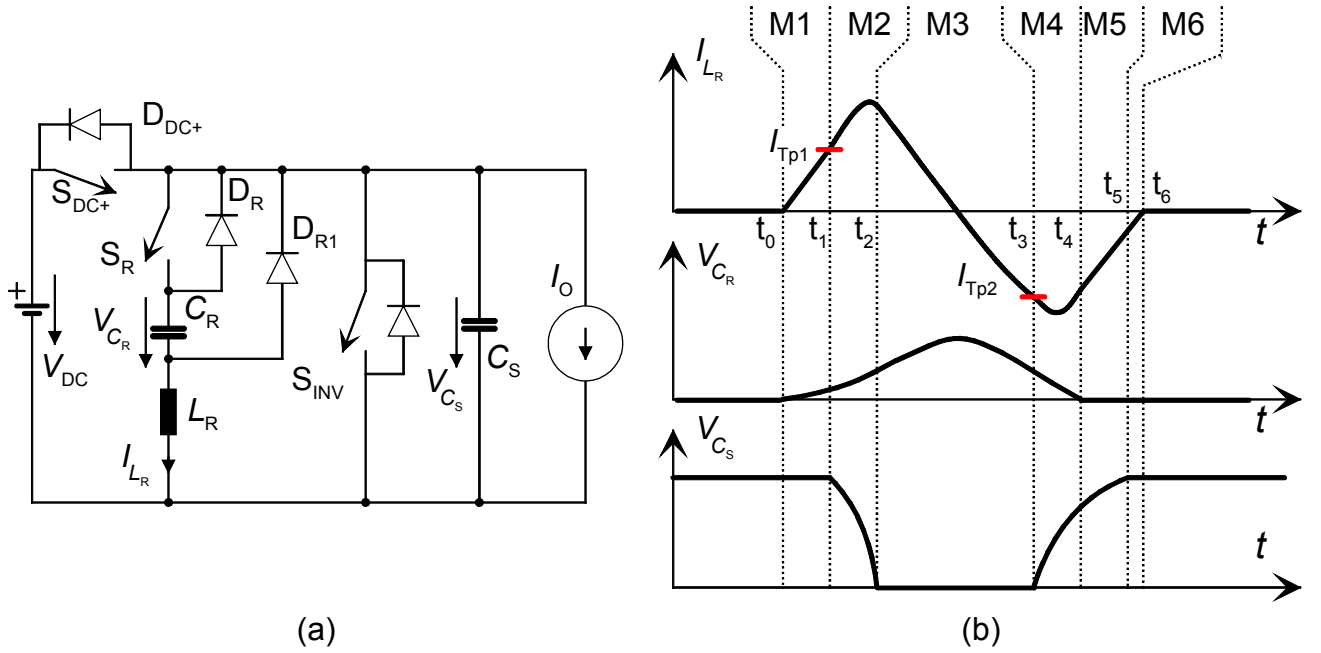


Figure 5.2: Simplified circuit for the T2 converter topology (a); Theoretical waveforms (b)

more complicated control requirements (complex circuit equations) due to three passive resonant elements in total. Next, the operation principle for both topologies will be detailed.

### 5.1.1 Principles of operation

The operation of both QR DC-link converters is based on the initiation of a resonant oscillation, which brings the voltage of the inverter bridge to zero. Thus, the ZVS condition is available for the inverter bridge switches to change the PWM state. Beside the passive elements for the energy storage, additional controlled switches, operated also under ZVS condition, are needed to initiate the resonant oscillation. Thus, the switching losses are considerably reduced. To analyze the resonant operation of each topology, following simplification is made: the inverter bridge is replaced by a single switch  $S_{INV}$ , modeling the short-circuit state of the inverter, a controlled current source  $I_O$ , which reflects the resulting load current at the DC-side of the inverter bridge and an equivalent parallel snubber capacitor  $C_S$  replacing the individual snubbers  $C'_S$ .

#### 5.1.1.1 Operation of converter topology T2

First, the simplified circuit of the T2 converter topology is drawn in Figure 5.2 (a) [70]. The related waveforms are shown in Figure 5.2 (b) and the different operation modes, (circuit individual states) from Figure 5.3, will be briefly presented together with the equations of the state variables. Thus, the analysis of the resonant operation is done step-by-step for each operation mode; the end conditions for one operation mode represent the initial conditions for the next one. Besides  $S_{DC+}$  and  $S_R$ , the diodes  $D_{DC+}$ ,  $D_R$  and  $D_{R1}$  allow the resonant current to freewheel. The equivalent current source  $I_O$  represents the DC-link current of the inverter, whose value and direction depends on the individual phase currents of the machine and the actual PWM state [71]. The value of this current is given by the following expression:

$$I_O = S_1 \cdot I_1 + S_3 \cdot I_2 + S_5 \cdot I_3, \quad \text{Eq. 5.1}$$

where  $S_1, S_3, S_5$  are the current state of the upper inverter switches (1 for turned on and 0 for turned off) and  $I_{1\div3}$  are the load currents with positive direction (from inverter to motor).

The state variables are: the inductor current  $i_{L_R}(t)$ , the voltage of the resonant capacitor  $v_{C_R}(t)$  and the voltage of the snubber capacitor  $v_{C_S}(t)$ .

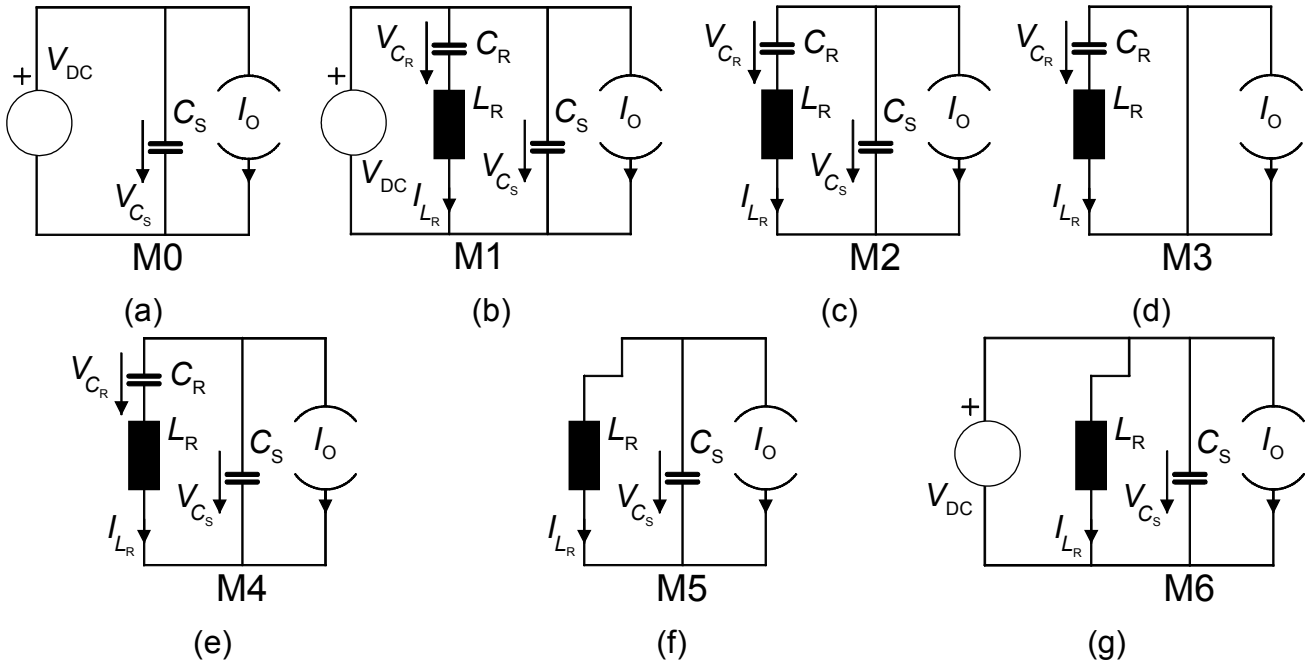


Figure 5.3: Operating modes for quasi-resonant converter topology T2

**Mode M0:** time interval before  $t_0$ 

The energy of the resonant circuit is zero in steady state, i.e. between the resonant operations. This corresponds to the circuit of mode M0 from Figure 5.3 (a) where the DC-link switch  $S_{DC+}$  is turned on and the resonant switch  $S_R$  is turned off. Thus, following equations are valid:

$$v_{C_R}(t) = 0; v_{C_S}(t) = V_{DC}; i_{L_R}(t) = 0.$$

Eq. 5.2

**Mode M1:** time interval between  $t_0$  and  $t_1$ 

The resonant cycle starts at  $t_0$  with the turn-on of the switch  $S_R$ , under ZCS condition. The resonant inductor  $L_R$  limits the current slope  $di_{L_R}/dt$  through  $S_R$ . Thus, the circuit for mode M1 is built (Figure 5.3 (b)) and  $L_R$  starts to be charged. Between the time instants  $t_0$  and  $t_1$ , following equations for the state variables are valid:

$$v_{C_R}(t) = V_{DC} \cdot [1 - \cos(\theta)]; v_{C_S}(t) = V_{DC}; i_{L_R}(t) = \frac{V_{DC}}{\sqrt{L_R/C_R}} \cdot \sin(\theta),$$

Eq. 5.3

where  $\theta = \omega_0 \cdot (t - t_0)$  represents the electrical angle. In this time interval, the resonant current rises following a sin function, while the voltage at the resonant capacitor increases with a (1-cos) function. Thus, the energy is stored in both resonant elements.

**Mode M2:** time interval between  $t_1$  and  $t_2$ 

As soon as the inductor current  $i_L$  reaches the trip current  $I_{Tp1}$  level, the switch  $S_{DC+}$  is turned off under ZVS conditions and the circuit for mode M2 is valid, see Figure 5.3 (c). This time instant is set by user and is very important to control the resonant operation. At this moment starts the resonance between  $L_R$ ,  $C_R$  and  $C_S$ , which ends with a zero-voltage condition for the inverter bridge  $v_{C_S}(t_2) = 0$ . The state variables are in this case:

$$v_{C_R}(t) = b[v_{C_R}(t_1) - V_{DC}] \cos(\theta) + [Z_3 i_{L_R}(t_1) + Z_4 I_O] \sin(\theta) + b \cdot V_{DC} + a \cdot v_{C_R}(t_1) - \frac{I_O(t - t_1)}{C_S + C_R};$$

$$v_{C_S}(t) = a[V_{DC} - v_{C_R}(t_1)] \cos(\theta) - Z_1[a I_O + i_{L_R}(t_1)] \sin(\theta) + b \cdot V_{DC} + a \cdot v_{C_R}(t_1) - \frac{I_O(t - t_1)}{C_S + C_R};$$

$$i_{L_R}(t) = [i_{L_R}(t_1) + a \cdot I_O] \cdot \cos(\theta) + \frac{V_{DC} - v_{C_R}(t)}{Z_2} \cdot \sin(\theta) - a \cdot I_O; \theta = \omega_1 \cdot (t - t_1).$$

Eq. 5.4



It can be noticed that the voltage of the snubber capacitor, which is the same as the inverter bridge voltage, starts to decrease. The initial conditions for the state variables are those from the time instant  $t_1$ . The resonant current and resonant capacitor voltage continue their resonance, following in this case Eq. 5.4.

**Mode M3:** time interval between  $t_2$  and  $t_3$

When the zero-voltage is obtained ( $v_{C_S}(t_2) = 0$ ), all the bridge switches are simultaneously turned on, under ZVS condition, which forces the clamping of the inverter bridge voltage to zero. Thus, the resonant current commutates to the freewheeling diodes of the inverter (circuit from Figure 5.3 (d) is valid), and the snubber capacitor  $C_S$  is no longer discharged. Turning on the inverter switches provides later a path for the resonant current to change its direction. The resonance between  $L_R$  and  $C_R$  decreases the inductor current, which becomes negative using following equations:

$$\begin{aligned} v_{C_R}(t) &= v_{C_R}(t_2) \cdot \cos(\theta) + \sqrt{L_R / C_R} \cdot i_{L_R}(t_2) \cdot \sin(\theta); \\ v_{C_S}(t) &= 0; \\ i_{L_R}(t) &= i_{L_R}(t_2) \cdot \cos(\theta) - \frac{V_{C_R}(t_2)}{\sqrt{L_R / C_R}} \cdot \sin(\theta); \quad \theta = \omega_0 \cdot (t - t_2). \end{aligned} \quad \text{Eq. 5.5}$$

When the voltage over the resonant capacitor reaches its maximum, the resonant current changes its direction and starts to discharge this capacitor. The current will flow now through the anti-parallel diode of  $S_R$ , namely  $D_R$ .

**Mode M4:** time interval between  $t_3$  and  $t_4$

The second important moment in the control of the resonant operation is when the resonant current reaches the level of the second trip current  $I_{Tp2}$ . Now, the new PWM state is set ( $S_{INV}$  turn off) under ZVS and the circuit for mode M4 is valid (Figure 5.3 (e)). The load current is changed to the new value  $I_{OX}$ , decided by this PWM state. The resonant current starts to charge the snubber capacitor  $C_S$ . Following equations are valid:

$$\begin{aligned} v_{C_R}(t) &= b \cdot v_{C_R}(t_3) \cos(\theta) + [Z_3 i_{L_R}(t_3) + Z_4 I_{OX}] \sin(\theta) + a \cdot v_{C_R}(t_3) - \frac{I_{OX}(t - t_3)}{C_S + C_R}; \\ v_{C_S}(t) &= a \cdot v_{C_R}(t_3) \cdot [1 - \cos(\theta)] - Z_1 [a I_{OX} + i_{L_R}(t_3)] \cdot \sin(\theta) - \frac{I_{OX}(t - t_3)}{C_S + C_R}; \\ i_{L_R}(t) &= [i_{L_R}(t_3) + a \cdot I_{OX}] \cdot \cos(\theta) - \frac{V_{C_R}(t_3)}{Z_2} \cdot \sin(\theta) - a \cdot I_{OX}; \quad \theta = \omega_1 \cdot (t - t_3). \end{aligned} \quad \text{Eq. 5.6}$$

**Mode M5:** time interval between  $t_4$  and  $t_5$

During the charge process of the snubber capacitor  $C_S$ , the voltage on the resonant capacitor  $C_R$  drops to zero. Thus, the resonant current changes its path, starting to flow through the auxiliary diode  $D_{R1}$ , see the equivalent circuit for mode M5 from Figure 5.3 (f). The elimination of  $C_R$  from the circuit simplifies the equations for the state variables:

$$\begin{aligned} v_{C_R}(t) &= 0; \\ v_{C_S}(t) &= v_{C_S}(t_4) \cdot \cos(\theta) - Z_5 \cdot [i_{L_R}(t_4) + I_{OX}] \cdot \sin(\theta); \\ i_{L_R}(t) &= [i_{L_R}(t_4) + I_{OX}] \cdot \cos(\theta) + \frac{v_{C_S}(t_4)}{Z_5} \cdot \sin(\theta) - I_{OX}; \quad \theta = \omega_2 \cdot (t - t_4). \end{aligned} \quad \text{Eq. 5.7}$$

**Mode M6:** time interval between  $t_5$  and  $t_6$

When the inverter bridge voltage reaches the level of the DC-link voltage  $V_{DC}$ , the freewheel diode  $D_{DC+}$  becomes forward biased and the excess resonant energy is transferred back to the DC-link capacitor. Thus, the circuit from Figure 5.3 (g) is valid.  $S_{DC+}$  is turned on under ZVS conditions. The state variables are in this case:

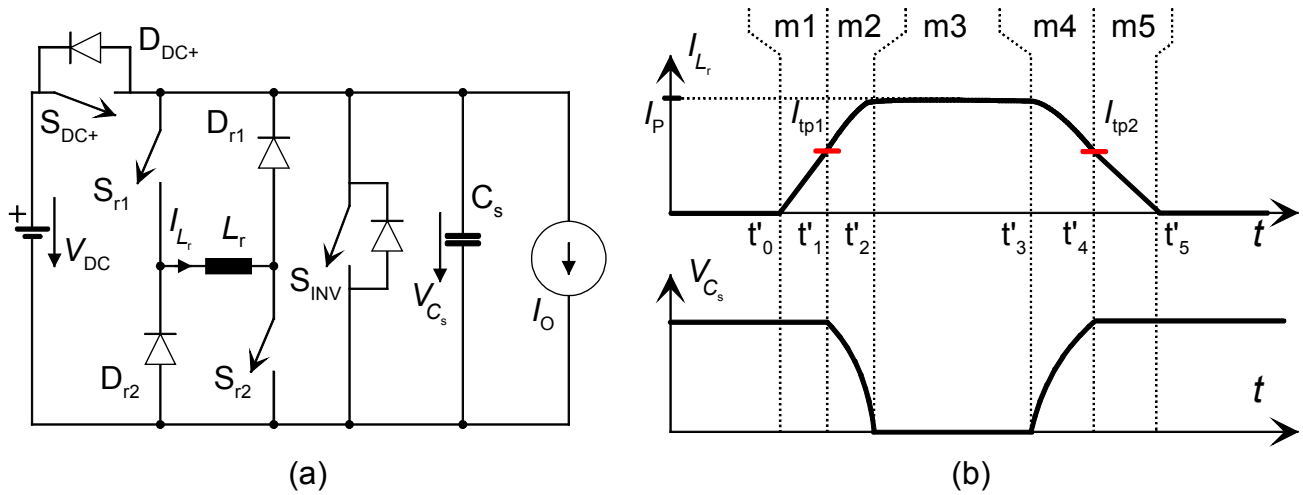


Figure 5.4: Simplified circuit of converter topology T1 (a); Theoretical waveforms (b)

$$v_{C_R}(t) = 0; v_{C_s}(t) = V_{DC}; i_{L_r}(t) = i_{L_r}(t_5) + \frac{V_{DC}}{L_R} \cdot (t - t_5). \quad \text{Eq. 5.8}$$

A linear increase of the resonant current is observed, approaching the zero value. This indicates the shift of the remaining energy from the resonant circuit to DC link. This mode ends with the steady-state values of the state variables; further, the new PWM switching state of the inverter-bridge is active. Thus, the change of the PWM state is realized only under ZCS and ZVS conditions, eliminating the switching losses.

Following notations were used to simplify the presentation of equations:

$$\omega_0 = \frac{1}{\sqrt{L_R C_R}}; \omega_1 = \sqrt{\frac{C_S + C_R}{L_R C_S C_R}}; \omega_2 = \frac{1}{\sqrt{L_R C_S}}; a = \frac{C_R}{C_S + C_R}; b = \frac{C_S}{C_S + C_R};$$

$$Z_1 = \frac{1}{\omega_1 C_S}; Z_2 = \omega_1 L_R; Z_3 = \frac{1}{\omega_1 C_R}; Z_4 = \frac{1}{\omega_1 (C_S + C_R)}; Z_5 = \sqrt{\frac{L_R}{C_R}}.$$

### 5.1.1.2 Operation of converter topology T1

Next, the topology T1 is analyzed. Its simplified circuit, shown in Figure 5.4 (a), contains the same switch \$S\_{INV}\$ that simulates the entire inverter bridge. The inductor \$L\_r\$ and capacitor \$C\_s\$ are used as resonant elements to store the energy during the resonant cycle. In this case only two state variables are involved: the resonant current \$i\_{L\_r}(t)\$ and snubber capacitor voltage \$v\_{C\_s}(t)\$. The waveforms of the resonant operation are shown in Figure 5.4 (b). As already mentioned, the less number of resonant elements (here only two) determine simpler analysis and less operation modes. Besides the resonant switches \$S\_{r1}\$ and \$S\_{r2}\$, the diodes \$D\_{r1}\$ and \$D\_{r2}\$ allow the resonant current to freewheel. The equivalent current source \$I\_O\$ represents the inverter DC-link current, whose value and direction depends on the individual phase currents of the machine and the actual PWM state [71]. Like in the previous case, the DC-link current before the resonant cycle is \$I\_O\$ and after, \$I\_{OX}\$.

The following abbreviations will be used in the equations:

$$\omega_r = \frac{1}{\sqrt{L_r C_s}}; Z_r = \sqrt{\frac{L_r}{C_s}}.$$

#### Mode m0: time before \$t'\_0\$

The energy of the resonant circuit is zero in the steady state, i.e. between the resonant operations. This corresponds to the circuit for mode M0 from Figure 5.5 (a) where the DC-

link switch  $S_{DC+}$  is turned on and resonant switches  $S_{r1}$  and  $S_{r2}$  are turned off. Thus, following equations are valid:

$$v_{C_s}(t) = V_{DC}; i_{L_r}(t) = 0.$$

Eq. 5.9

**Mode m1:** time between  $t'_0$  and  $t'_1$

When a change of the PWM state is needed, the resonance operation is initiated by closing the switches  $S_{r1}$  and  $S_{r2}$  under ZCS condition. The simplified circuit from Figure 5.5 (b) is obtained where it can be noticed, that the resonant current begins to increase linearly until the trip current  $I_{tp1}$  is reached (see Figure 5.4 (b)). By choosing the trip current level  $I_{tp1}$ , the amount of energy stored during the resonant cycle can be adjusted. Similar to the operation mode M1 from the converter topology T2, this mode controls the resonant cycle. The equations for the state variables are:

$$v_{C_s}(t) = V_{DC}; i_{L_r}(t) = \frac{V_{DC}}{L_r} \cdot (t - t'_0).$$

Eq. 5.10

**Mode m2:** time between  $t'_1$  and  $t'_2$

When the resonant current reaches  $I_{tp1}$ ,  $S_{DC+}$  is turned off, under ZVS condition, resulting in the simplified circuit from Figure 5.5 (c). Due to the resonance between  $L_r$  and  $C_s$  the voltage of the inverter-bridge drops to 0. The relations for state variables are:

$$v_{C_s}(t) = V_{DC} \cdot \cos(\theta) - Z_r \cdot [I_{tp1} + I_O] \cdot \sin(\theta);$$

$$i_{L_r}(t) = [I_{tp1} + I_O] \cdot \cos(\theta) + \frac{V_{DC}}{Z_r} \cdot \sin(\theta) - I_O; \theta = \omega_r \cdot (t - t'_1).$$

Eq. 5.11

The end value of the resonant inductor current  $I_P$  represents the maximum resonant current [69] and determines the energy stored during the resonant cycle:

$$I_P = i_{L_r}(t'_2) = \sqrt{(I_{tp1} + I_O)^2 + (V_{DC} / Z_r)^2} - I_O.$$

**Mode m3:** time between  $t'_2$  and  $t'_3$

After the voltage of the inverter-bridge reaches 0V, the switch  $S_{INV}$  is turned on to force the voltage clamping to zero. The resulting simplified circuit is drawn in Figure 5.5 (d). The resonant current freewheels through the following paths:  $S_{r1} \rightarrow D_{r1}$  and  $S_{r2} \rightarrow D_{r2}$ . The state variables have the following expressions:

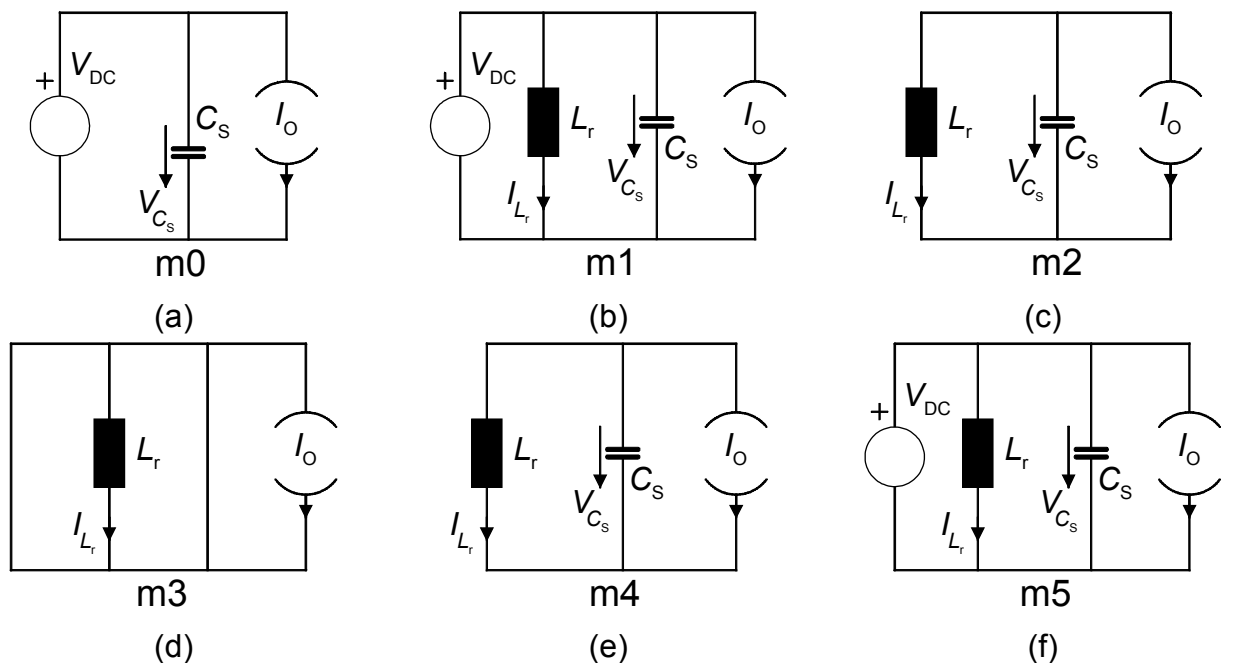


Figure 5.5: Operating modes for quasi-resonant converter topology T1

$$v_{C_s}(t) = 0; i_{L_r}(t) = I_P. \quad \text{Eq. 5.12}$$

Theoretically, the resonant current maintains its constant value  $I_P$ , but in reality it decreases due to losses. Therefore, the choice of the trip current  $I_{tp1}$  is important to store enough energy in the resonant elements in order to allow the restoration of the inverter bridge voltage back to the DC-link level. At the end of this time interval the next PWM state is activated ( $S_{INV}$  is turned off) under ZVS condition. This determines the DC-link current  $I_O$  to change its value to  $I_{OX}$ , corresponding to the next PWM state, see Eq. 5.1.

**Mode m4:** time between  $t'_3$  and  $t'_4$

Right after the next PWM state is activated, both resonant switches,  $S_{r1}$  and  $S_{r2}$ , are turned off under ZVS condition. Thus, a path through the freewheel diodes  $D_{r1}$  and  $D_{r2}$  is created for the resonant current to charge the snubber capacitor  $C_s$ , see the simplified circuit from Figure 5.5 (e). The state variables equations are as follows:

$$\begin{aligned} v_{C_s}(t) &= Z_r \cdot (I_P - I_{OX}) \cdot \sin(\theta); \\ i_{L_r}(t) &= (I_P - I_{OX}) \cdot \cos(\theta) + I_{OX}; \quad \theta = \omega_r \cdot (t - t'_3). \end{aligned} \quad \text{Eq. 5.13}$$

The inverter bridge voltage reaches the DC-link level at the end of this operation mode and the resonant current is equal to the second trip current  $I_{tp2}$ :

$$I_{tp2} = i_{L_r}(t'_4) = \sqrt{(I_P - I_{OX})^2 - (V_{DC} / Z_r)^2} + I_{OX}.$$

This value determines the energy left in the inductor at the end of **Mode m4**.

**Mode m5:** time between  $t'_4$  and  $t'_5$

After the snubber capacitor is complete charged, the remaining energy ( $I_{tp2}$ ) in the resonant inductor is returned to the DC link via freewheel diode  $D_{DC+}$ , see the simplified circuit from Figure 5.5 (f). The switch  $S_{DC+}$  can be turned on again under ZVS condition, while the anti-parallel diode  $D_{DC+}$  is conducting. The inverter bridge voltage remains constant while the resonant current decreases linearly to the zero value:

$$v_{C_s}(t) = V_{DC}; i_{L_r}(t) = -\frac{V_{DC}}{L_r} \cdot (t - t'_4) + I_{tp2}. \quad \text{Eq. 5.14}$$

This mode ends with the steady-state values for state variables; further, the new PWM switching state of the inverter bridge is active. Similar to the T2 topology case, the change of the PWM state is realized only under ZCS and ZVS conditions, eliminating the switching losses.

Finally, comparing the sets of equations between the converter topology T1 (Eq. 5.9 to Eq. 5.14) and converter topology T2 (Eq. 5.2 to Eq. 5.8), it can be noticed that the absence of the resonant capacitor  $C_R$  simplifies the equations. However, topology T2 was found to have lower losses than topology T1 because the energy is shared between the resonant inductor and the resonant capacitor.

### 5.1.2 Efficient operation – optimal energy use for resonant operation

For the QR DC-link converter topologies presented in the literature, typically a larger than necessary amount of energy is stored in the resonant elements to allow a safe margin for the inverter voltage to restore to the DC-link level. In fact, this additional energy storage leads naturally to power losses inside the resonant elements. A different control strategy for the resonant operation, first mentioned in [69], allows storing only the minimum amount of energy in the resonant circuit, needed to restore the inverter-bridge voltage back to the DC-link level. For that, a fast control has to be implemented using, e.g. Field Programmable Gate Arrays (FPGA), as the resonant cycle needs to be controlled fast.

Starting from topology T2, the aim is to calculate the trip currents  $I_{Tp1}$  and  $I_{Tp2}$  for all the load currents such that [72]:

- at the end of the resonant cycle the DC-link voltage is restored;
- the amplitudes of the resonant current are minimized.

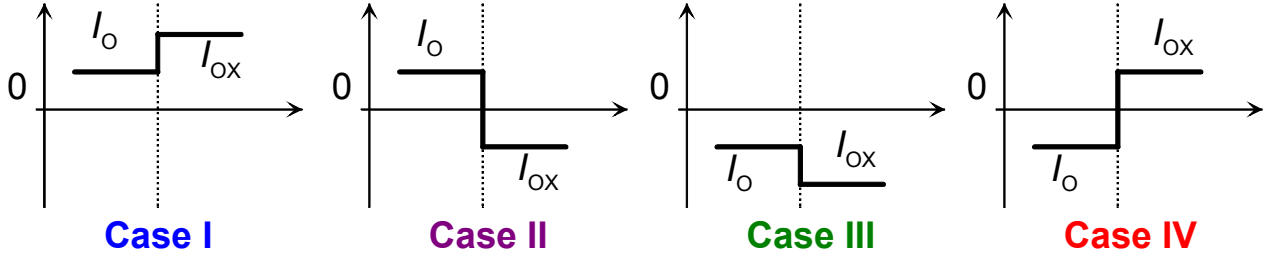


Figure 5.6: Change of the DC-link current from actual to next PWM state [72]

The resonant cycle is heavily influenced by the initial load current  $I_O$  and by the load current  $I_{OX}$  at the next PWM switching state, see Eq. 5.1. In order to get the general results for all combinations of  $I_O$  and  $I_{OX}$ , the analytical solutions for this boundary problem shall be used as far as possible.

The optimization method aims at the following: for each mode, the solutions for the state variables i.e. resonant inductor current and resonant capacitor voltage are derived, see Eq. 5.2 to Eq. 5.8. The problem is to find the boundaries between all the operation modes, such that all constraints are fulfilled. An analytical solution turned out to be either impossible or at least highly complicated for topology T2 due to the complex modes and all three passive elements:  $L_R$ ,  $C_R$  and  $C_S$ . Therefore, the problem is solved in two steps [72]:

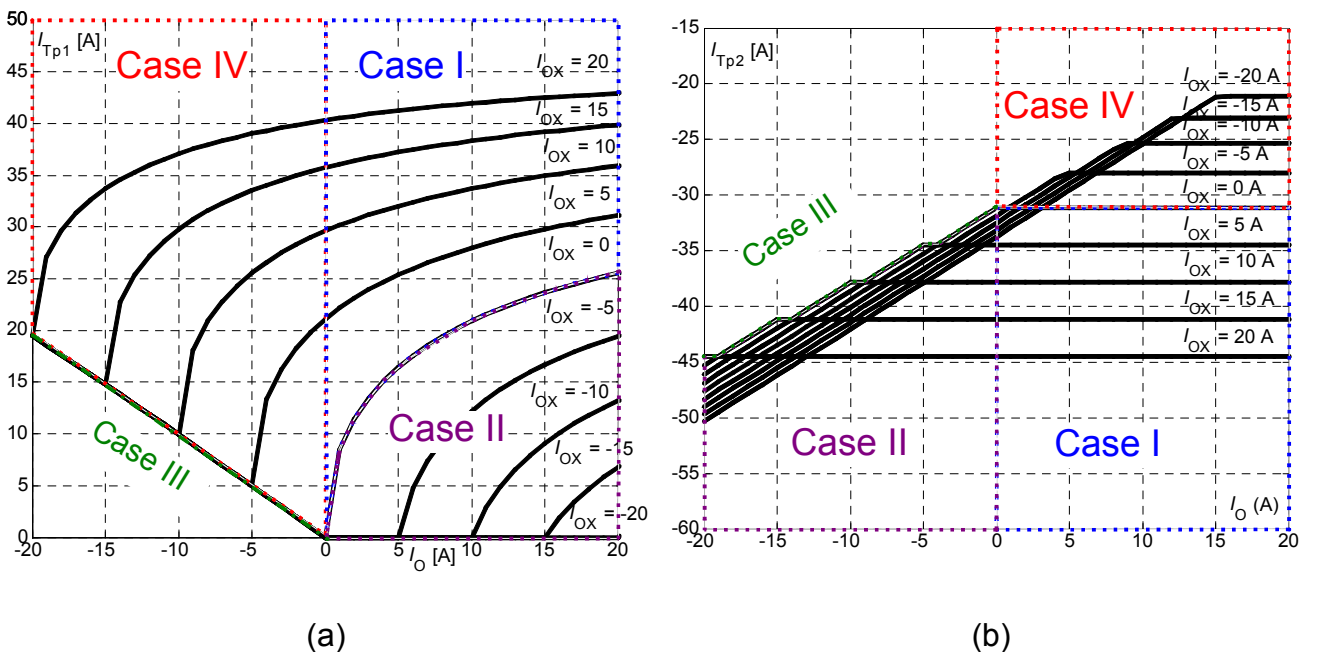
- first, the solution is derived for topology T1, having only one instead of two capacitors and less/simpler modes. From the obtained solutions, the energy stored in the resonant elements during mode m1 is calculated.

- second, storing the same amount of energy (Eq. 5.15) during mode M1 from topology T2, allows to calculate the trip current  $I_{Tp1}$ . In a similar way  $I_{Tp2}$  can be found from (Eq. 5.16). Therefore, the following assumption is important: in both converter topologies the values are the same for inductances  $L_R$ ,  $L_r$  and capacitances  $C_S$  and  $C_s$ , respectively.

$$1/2 \cdot C_R \cdot v_{C_R}^2(t_1) + 1/2 \cdot L_R \cdot I_{Tp1}^2 = 1/2 \cdot L_r \cdot I_{tp1}^2, \text{ with } i_{L_r}(t_1) = I_{Tp1}; i_{L_r}(t'_1) = I_{tp1}; \quad \text{Eq. 5.15}$$

$$1/2 \cdot C_R \cdot v_{C_R}^2(t_3) + 1/2 \cdot L_R \cdot I_{Tp2}^2 = 1/2 \cdot L_r \cdot I_{tp2}^2, \text{ with } i_{L_r}(t_3) = I_{Tp2}; i_{L_r}(t'_4) = I_{tp2}. \quad \text{Eq. 5.16}$$

Generally, the trip current is a function of inverter input current (DC-link current)  $I_O$  and other parameters. Because  $I_O$  changes its value and direction for the next PWM state according to Eq. 5.1, four different cases, classified by the direction of actual and next DC-


 Figure 5.7: Variation characteristic for optimal trip currents  $I_{Tp1}$  (a) and  $I_{Tp2}$  (b)

link currents, are illustrated in Figure 5.6: **Case I**  $\rightarrow I_{OX} = 2I_O > 0$ ; **Case II**  $\rightarrow I_{OX} = -I_O < 0$ ; **Case III**  $\rightarrow I_{OX} = 2I_O < 0$ ; **Case IV**  $\rightarrow I_{OX} = -I_O > 0$ .

Now, for each case, the trip currents  $I_{tp1}$  and  $I_{tp2}$  are calculated for the converter topology T1 using the equations defined by each individual mode, Eq. 5.9 to Eq. 5.14. Using the energy balance relations from Eq. 5.15 and Eq. 5.16, the trip currents for topology T2 are determined. The calculation procedure is described thoroughly in [72] and will not be detailed here. Figure 5.7 shows the optimal values of the trip currents for topology T2. It can be noticed that each case from Figure 5.6 leads to different trip current values. By knowing the characteristics in Figure 5.7 for both trip currents  $I_{Tp1}$  and  $I_{Tp2}$ , the optimal resonant operation is provided for all possible cases at a PWM state change only when the actual and the next values of the DC-link currents are measured and/or estimated by a fast logic unit, e.g. a FPGA.

### 5.1.3 Efficient operation – new family of semiconductor devices

The characteristics of the semiconductor switches are also important for the efficiency of the entire converter. Having a ZVS, the turn-on losses can be neglected. In this case, the conduction losses will be dominant. For that, a new IGBT Trench-Fieldstop 4<sup>®</sup> technology is used for the inverter bridge switches to minimize the conduction losses.

Much larger constraints are valid for the resonant switches than for the bridge switches, especially for  $S_{DC+}$ , see Figure 5.1 (b): they must switch very fast, around 100 kHz and at the same time have very low conduction losses, as they are supplying the energy from the DC link to inverter and are conducting most of the time. These switches are turned off only during the resonant cycle, which is much shorter than a PWM state period. Two available semiconductor types are found to be appropriate and will be further considered: CoolMOS field effect transistor [73] and Emitter-Switched Bipolar Transistor (ESBT) [74], [76].

The **CoolMOS** transistor [73] is suited for the high switching frequency and presents relative low conduction losses compared to the normal MOSFET transistors, but is available only up to 650 V blocking voltage. New products with 800-V blocking capability have been announced but they are not commercially available. The structure of a CoolMOS is shown in Figure 5.8 (a). The drain-source resistance  $R_{DS}$  is minimized by introducing the vertical  $n$  layer, which is higher doped than epitaxial  $n$  layer. Thus, the total  $R_{DS}$  is minimized using a larger quantity of electrons. The disadvantage remains the limited blocking voltage of 650 V, which makes them inappropriate to be used for the switch  $S_R$ . However, a safe margin is offered by the avalanche effect, allowing short overloading of the device and making it more robust. This was proved by measurements at

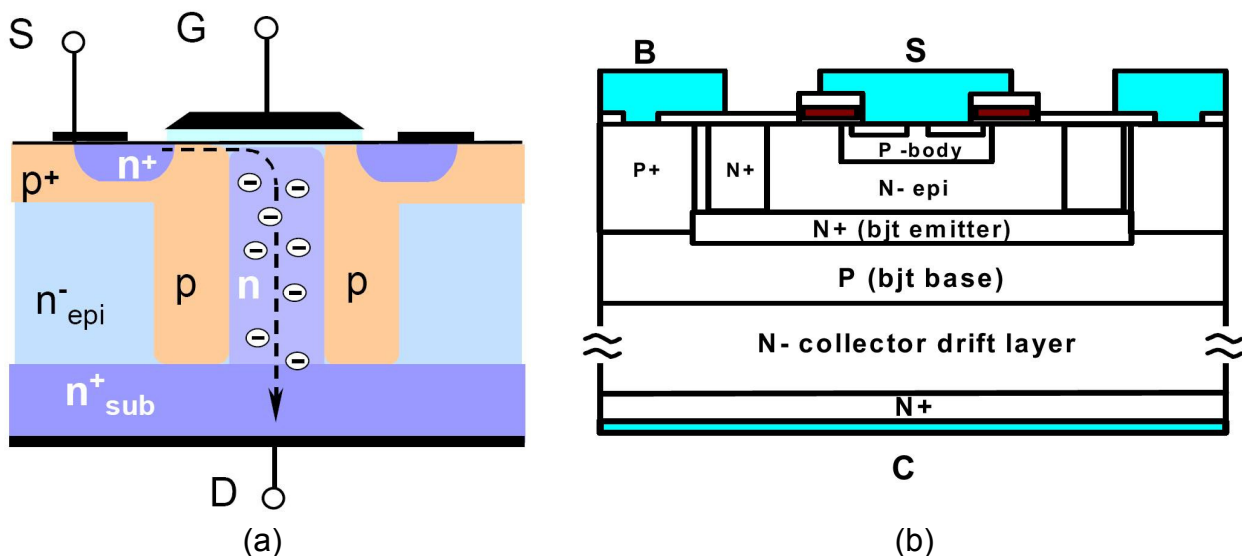
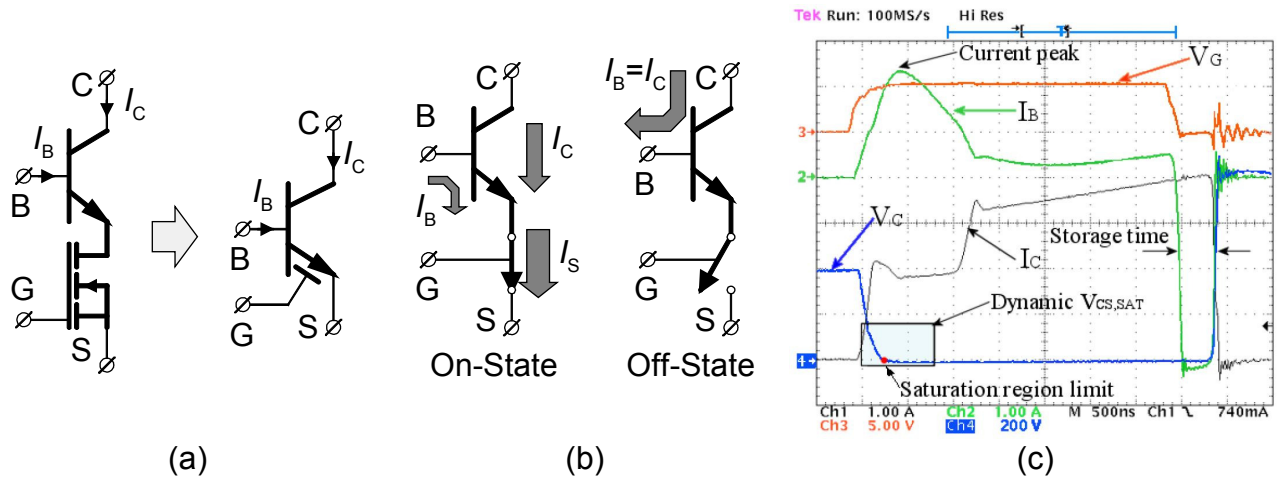


Figure 5.8: CoolMOS physical structure [73] (a); ESBT physical structure [77] (b)



**Figure 5.9: ESBT symbol (a), current flow for on/off states (b); standard switching waveforms (c) [74]**

a small setup where short voltage overshoots did not destroy the device. Of course the producer does not recommend the device operation under such conditions.

The second device analyzed, the **ESBT**, combines the low conduction losses of the bipolar structure with the fast-switching transients of the FET structure into a monolithic cascode connection. The symbol is illustrated in Figure 5.9 together with the standard switching waveforms and the current flow through the switch for both operation modes [74]. The ESBT has a four-pin structure making the drive circuits more complex as for IGBT or MOSFET. While the FET part can be supplied from a standard PWM driver, a special driver for the bipolar part has to supply the base current  $I_B$ .

In the vertical structure, shown in Figure 5.8 (b), the BJT part can be recognized at the collector side, forming the *npn* structure. The lowly doped epitaxial *n*<sup>-</sup> layer of the FET neighbors directly the buried BJT emitter *n*<sup>+</sup> layer. The channel is built in the FET p-body layer, allowing electrons to flow from source to the BJT emitter *n*<sup>+</sup> layer. When current is injected to the BJT base through the fourth pin (B), the ESBT starts to conduct.

First, as claimed by the producer, the ESBT advantages are:

- a) small voltage drop during on state (e.g. 1.3V for STE50DE100) due to the bipolar structure (the FET part is designed for small voltages and therefore has small  $R_{DS}$ );
- b) high blocking voltages are possible due to the bipolar part;
- c) relative fast switching times compared to IGBT are possible when appropriate drivers are used.

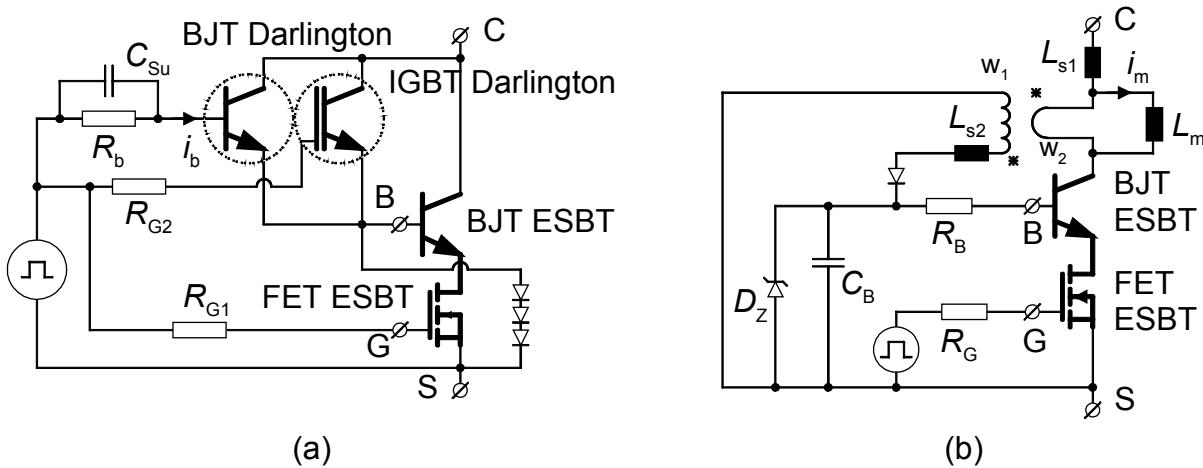
However, complex drivers are needed to obtain good dynamic performances of the ESBT bipolar structure.

Further, the switching transition from Figure 5.9 (c) is analyzed:

- at **turn-on**, the FET switches very fast and creates a path for the collector current  $I_C$ . The collector-source voltage  $V_{CS}$  drops to zero, having a specific delay determined by the initial value of the base current. This effect is also called “dynamic saturation”. A high base current  $I_B$  must therefore be impressed to the base to accelerate the turn-on process. However, a high base current level will determine a low level for the collector current  $I_C$ , immediately after turn-on transient. Only when  $I_B$  reaches the steady-state value,  $I_C$  is close to the source current  $I_S$ ;
- at **turn-off**, the FET cuts the path for  $I_C$ . The only available path remains through the ESBT basis, that is why during this time, also called “storage time”,  $I_B = -I_C$ , see Figure 5.9 (b). In other words, the carriers trapped in the p-base region of the BJT part (see Figure 5.8 (b)) must be evacuated as fast as possible to assure a quick turn-off transient.

As already mentioned, the ESBT is more complicated to drive compared to IGBT, due to the presence of the bipolar part, that has to be supplied with constant base current. Therefore two driver circuits, shown in Figure 5.10, are analyzed and tested later, see subchapter 5.2. In the first driver, the base current is supplied by a Darlington connection





**Figure 5.10: Darlington-type driver (a) and proportional-type driver (b)**

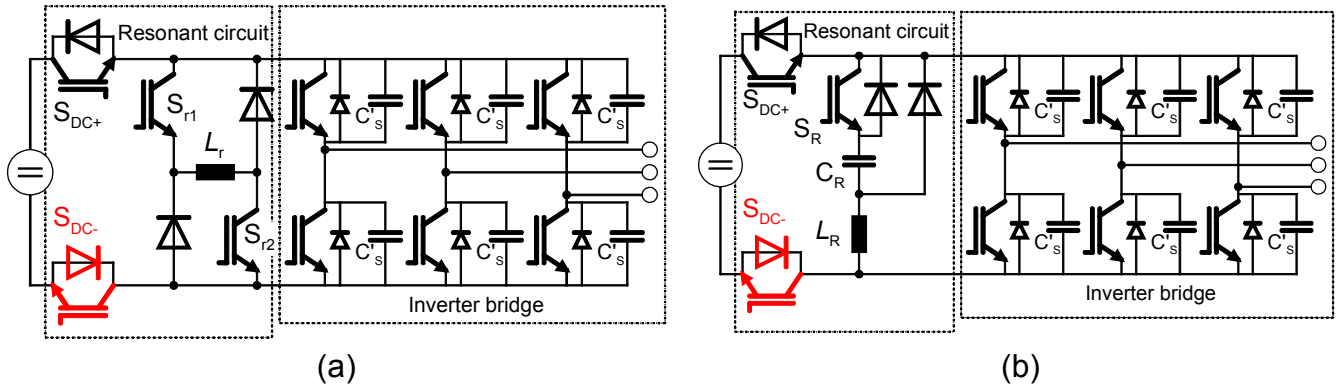
consisting of a BJT transistor in parallel with an IGBT [75], see Figure 5.10 (a). The Darlington IGBT and the FET part of the ESBT provide the high  $I_B$  peak value for the ESBT turn on, whereas the Darlington BJT is responsible for low voltage during the on state. Yet, the Darlington BJT has to block the entire voltage of ESBT. It is well known that, high blocking voltage capability is obtained at bipolar devices only with large base area, leading further to low values for the amplification factor  $h_{FE}$ . That is why, relative high base currents are necessary to maintain the Darlington BJT saturated. This determines an undesired increase of the driver losses. Moreover, when larger  $I_C$  pulses are required for a small period of time, like in the resonant operations, the BJT part may come out of saturation, due to the limited base current from the Darlington BJT. Therefore, the conduction losses increase. The Darlington IGBT and FET part of ESBT use the resistances  $R_{G2}$  and  $R_{G1}$  to limit the gate currents. The base current for Darlington BJT is kept to a constant value using the resistance  $R_b$ . The transient dynamic can be improved adding the capacitance  $C_{Su}$  in parallel to  $R_b$ . Several series-connected diodes are protecting the base – source connection of the ESBT from overvoltages.

The second driver topology from Figure 5.10 (b), also called “proportional-type driver”, uses a pulse transformer to supply a base current proportional to the collector current [75]. This will work also for high pulse currents. Due to the reversed winding signs of the pulse transformer, a negative  $I_C$  current slope determines the loading of the capacitor  $C_B$ , thus preparing the ESBT for the next turn-on. When this command occurs, the FET is turned on first, allowing the capacitor to deliver the base current. The resistor  $R_B$  limits the peak of the base-current. An undesired discharge of  $C_B$  via secondary winding of the pulse transformer is avoided by a diode. Additional, a Zener diode  $D_Z$  protects the base–source ESBT connection. The drawback of such driver is the need to demagnetize the pulse transformer, which makes it difficult to implement for the  $S_{DC+}$  switch of the QR converter. The on-state period of this switch is much longer than the off-state period and, therefore, additional demagnetization paths have to be provided.

The fourth **IGBT** generation (Trench Fieldstop 4<sup>®</sup>) has also been investigated [78]. They combine the advantage of the trench-gate technology (low on-state voltage) with the fast switching capabilities of the field-stop technology, making them suitable for switching frequencies up to 30kHz. Still, IGBT Trench Fieldstop 4<sup>®</sup> possess large turn-off delay due to the trench-gate technology (poor transient dynamic). For example, such IGBTs can be used for the resonant switch  $S_R$  because, as seen in Figure 5.2 (b), the turn-off delay is not critical for the resonant cycle during the operation mode M3 ( $S_R$  can be turned off between the time instant where the resonant current is crossing zero and the end of mode M3).

Other competitive switching semiconductor devices, applicable for the resonant switches, are the **SiC JFETs** [65]. They are suitable for fast switching, have low switching losses and are able to block voltages of 1200 V or even higher. As such devices are





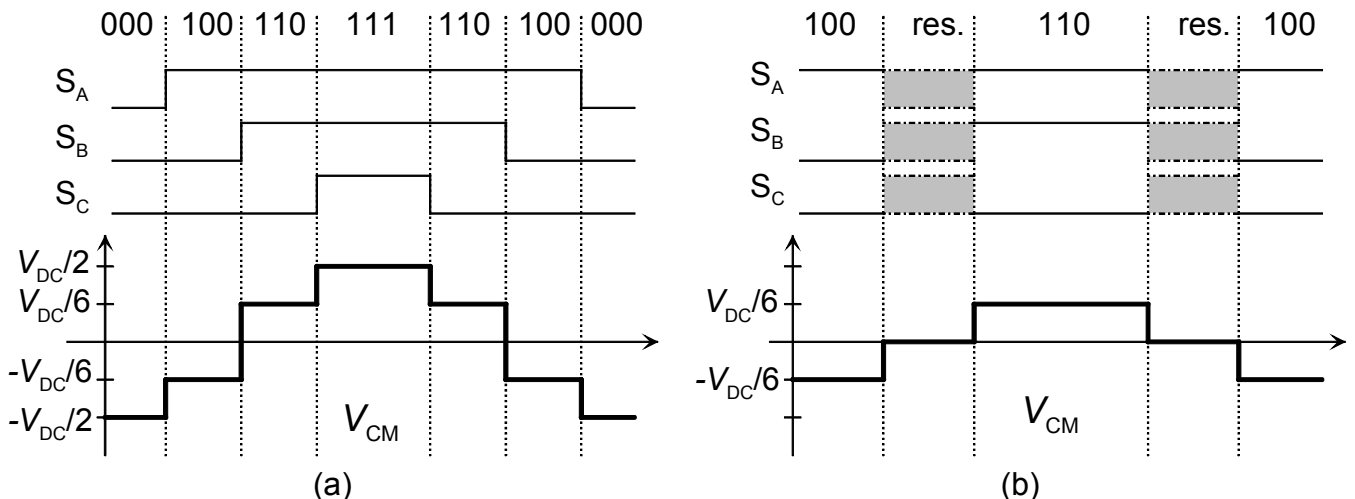
**Figure 5.11: Circuit modification for reduction of common-mode voltage at topology T1 (a) and T2 (b)**

presently not commercially available, they can be the subject of a future research and optimization for the resonant converters.

#### 5.1.4 Motor-friendly characteristics

Beside the energy efficiency of the converter, achievable with an optimal control of the resonant cycle and new semiconductor devices, the aspect of the motor-friendliness of the converter is very important when long cables are used. As already presented, the inverter output voltage during the resonant cycle drops to zero, whereas the voltage slope is smoothed by the passive elements of the resonant circuit ( $L_R$ ,  $C_R$  and  $C_S$ ) and depends no longer on the hard-switching behavior of the semiconductors. Thus, harmless voltage gradients, dependent on cable length, can be obtained. As it will be shown in the next subchapter, the voltage slope was limited to 600 V/ $\mu$ s for the 34 m long LAPP shielded cable. This corresponds to a voltage overshoot at motor terminals of less than 20%. A compromise remains to be achieved between the desired voltage gradient and the possible modulation index: the smaller the voltage gradient is, the longer time is needed for the resonant cycle to assure these small gradients. But longer resonant operations diminish the active period inside a PWM state, which leads finally to smaller possible modulation indexes.

Additional to the reduction of the voltage slope by means of resonant passive elements, the reduction of common-mode (CM) voltage  $V_{CM}$  is proposed by inserting a second DC-link switch  $S_{DC-}$ , as shown in Figure 5.11, to completely separate the inverter from the DC link for both T1 and T2 converter topologies. It is well known in literature that, the CM voltage is responsible for the electrostatic discharge of the bearing capacities, leading further to large repetitive EDM bearing currents and finally fast bearing wear [16]. Therefore, a different modulation scheme has to be adopted so that the resonant operation



**Figure 5.12: Sine-triangle modulation (a) and DSC-like modulation (b)**

can be used as a zero-voltage period for the PWM modulation.

In Figure 5.12, two different modulation techniques are compared, i.e. the sine triangle modulation (Figure 5.12 (a)) and second a modulation where the zero vector, generated during the resonant cycle, follows each active vector (Figure 5.12 (b)). The latter is similar to the switching sequence from the “Direct Self Control” (DSC) modulation technique [79]. When using only  $S_{DC+}$  switch, all inverter outputs are short-circuited and connected to the minus DC-link bus during the resonant cycle, which determines the following CM voltage level:  $V_{CM} = -V_{DC}/2$ . By inserting an additional switch to separate also the minus DC-link bus,  $V_{CM}$  is canceled. Thus, only during PWM periods, when an active voltage vector is selected, will the CM voltage have the maximum level  $V_{CM} = \pm V_{DC}/6$ . The theoretical CM voltage curve, for both modulation methods, is shown also in Figure 5.12.

## 5.2 Hardware setup design and implementation

In this subchapter, the steps for the design and realization of the quasi-resonant converter will be briefly detailed together with the specific problems for the resonant operation. Starting with the selection of the semiconductor device, the converter design needs to fulfil more constraints regarding the motor friendly characteristic, which is the most important aspect in this work. Thus, the passive elements must be chosen carefully. Also, the implementation of the control unit will be briefly described together with the control scheme. Finally, the resulting hardware layout and system is presented.

### 5.2.1 Analysis of the semiconductor and converter topology

The characteristics of the semiconductor switches are important for the efficiency of the entire converter. Having ZVS and ZCS operation condition, the conduction losses will be dominant. Therefore, the new IGBT technology Trench-Fieldstop 4<sup>®</sup> is used for the inverter-bridge switches to minimize the conduction losses. Much larger constraints are valid for the resonant switches, especially for  $S_{DC+}$ ,  $S_{DC-}$  and  $S_R$  ( $S_{r1}$  and  $S_{r2}$ , respectively): they have to switch very fast, around 100 kHz, and, in the same time, to have very low conduction losses, because they are supplying the energy from the DC link to the inverter, conducting most of the time.

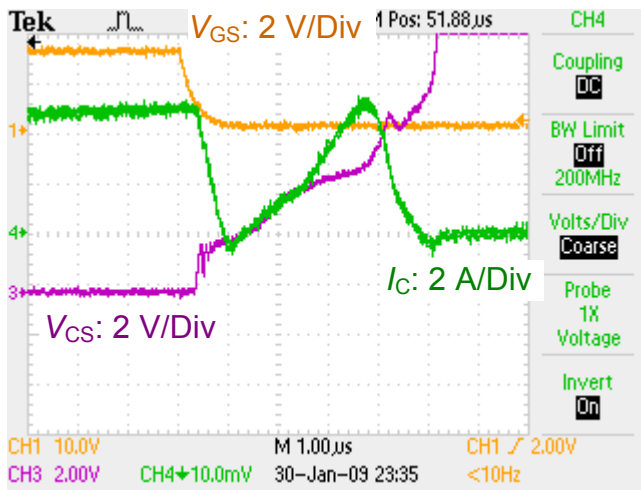
An investigation was conducted in [80] to compare the characteristics of the three different types of semiconductors from section 5.1.3: CoolMOS, Emitter-Switched Bipolar Transistor (ESBT) and IGBT 4<sup>th</sup> generation. Table 5.1 shows the data for the chosen devices regarding the nominal current  $I_N$ , the breakdown voltage  $V_{BR}$ , conduction losses of the DC-link switches  $S_{DC+}$  /  $S_{DC-}$  and conduction losses of the resonant switch  $S_R$ . These conduction losses were calculated considering a constant load current of 20A.

**Table 5.1: Data and conduction losses for the considered semiconductor devices [80]**

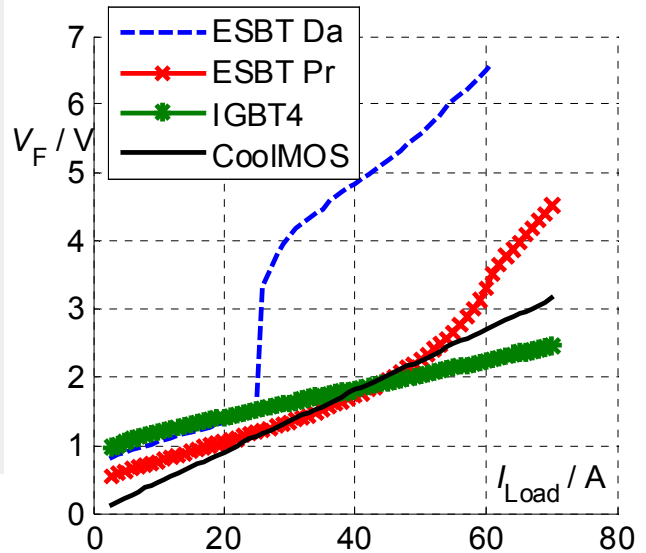
Semiconductor type	Device No.	$I_N$ / A	$V_{BR}$ / V	$P_{cond.} / W$ ( $I_{Load} = 20 / A$ ) $S_{DC+}$ or $S_{DC-}$	$P_{cond.} / W$ ( $I_{Load} = 20 / A$ ) $S_R$
ESBT	STE50DE100	50	1000	Darlington driver: 31.4	Darlington driver: 17.9
				proportional driver: 17.7	proportional driver: 7
CoolMOS	IPW60R045	60	650	17.8	-
IGBT <sup>4</sup>	IRG4PH50	57	1200	24.6	7.5

**Table 5.2: Semiconductor comparison for resonant-switch application**

CoolMOS	ESBT	IGBT 4 <sup>th</sup> generation
<b>Advantages:</b> + reduced switching losses + high switching frequency <b>Disadvantages:</b> – limited breakdown voltage levels – high parasitic output capacitance	<b>Advantages:</b> + high breakdown voltage levels + low conduction losses + relative small switching times <b>Disadvantages:</b> – complex driver circuitry	<b>Advantages:</b> + high breakdown voltage levels + low conduction losses <b>Disadvantages:</b> – large turn-off delay
Suited for DC-link switches $S_{DC+}$ and $S_{DC-}$ due to fast switching transitions	Improper for resonant operation due to complex gate circuitry and base current behavior (bipolar part) under ZVS switching condition	Suited for resonant switch $S_R$ due to reduced conduction losses and high-voltage blocking capability



(a)



(b)

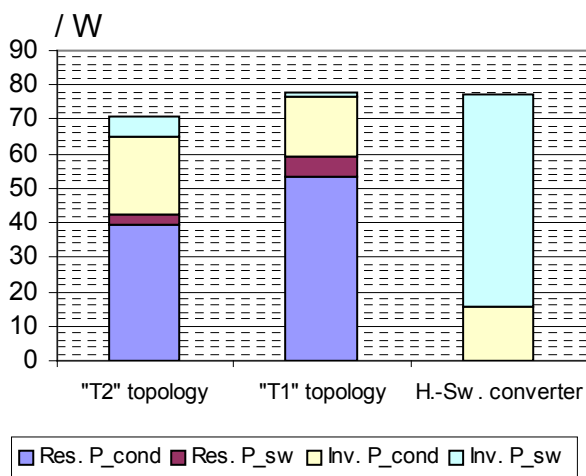
**Figure 5.13: Delayed ESBT turn-off transient under ZVS (a) [80]; voltage-current characteristics (b)**

According to the manufacturers, the ESBT should be suitable for the resonant operation [81]. However, when testing it under soft switching conditions several problems occurred:

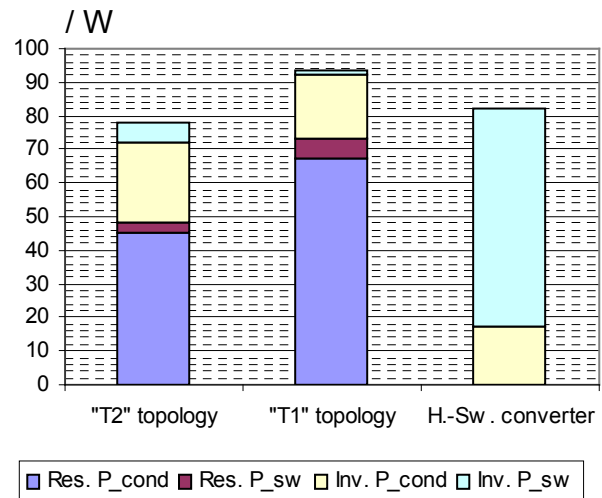
- maintaining the switch turned off with the zero collector-source voltage is difficult because the base-connected capacitance  $C_B$  discharges over the base-collector diode of the BJT part, see Figure 5.10 (b);
- turn off with reduced losses leads to a delay of collector current  $I_C$ , see Figure 5.13 (a);
- a Darlington driver circuit increases the conduction losses considerably, specially if the Darlington BJT comes out of the saturation due to the high base current  $I_B$  and shares it with the Darlington IGBT, see Figure 5.10 (a).

In conclusion the ESBT was found inappropriate for this application due to too high driver requirements. Complex drivers may solve the problems listed above, but the increasing cost and complexity will not be acceptable. The on-state voltage drop as a function of load current is shown in Figure 5.13 (b) for all three devices. The ESBT is considered being driven with both Darlington-type (ESBT Da) and proportional-type (ESBT Pr) driver circuits from Figure 5.10.

The CoolMOS represents a good solution by combining both high switching speed and low conduction losses. Due to its limited breakdown voltage (650 V), the CoolMOS can be



(a)



(b)

**Figure 5.14: Semiconductor losses for 2.8 kW motor load (a) and 3.5 kW motor load (b)**

used only for the DC-link separation switches  $S_{DC+}$  and  $S_{DC-}$ . Here, the entire DC-link voltage is shared between both switches. For the resonant switch  $S_R$ , the IGBT Trench-Fieldstop 4<sup>®</sup> is suitable due to the low conduction losses and high blocking voltage (1200 V). Moreover, the high delay (app. 500 ns for the selected device) is not critical in topology T2 as the turn-off time instant for  $S_R$  occurs between time instant where resonant current is crossing the zero value and end of mode M3. This does not affect the resonant cycle, see Figure 5.2 (b). Finally, Table 5.2 summarizes the evaluations and conclusions.

After selecting the semiconductor devices, the switching and conduction losses were roughly estimated for both quasi-resonant converter topologies. By including the on-state resistance  $R_{DS}$  for  $S_{DC+}$  and  $S_{DC-}$  (CoolMOS) and the on-state voltage  $V_{CEon}$  of  $S_R$  and all six inverter switches  $S_{1-6}$  (IGBT), the conduction losses are estimated from the simulation models. As a rule of thumb, the switching losses for the resonant operation ( $P_{sw}$ ) are roughly assumed to be 10% of conduction losses ( $P_{cond}$ ), as they are difficult to estimate. The switching and the conduction losses (hard-switching operation) for the 6-pack inverter are taken from the data sheet. Mrs. Kedarisetti estimated the total losses in the design stage of the QR DC-link converter. They are compared in Figure 5.14 for two points of load operation. It is clear that the converter topology T2 presents a slight advantage compared to T1, explained by a lower number of resonant switches required for the resonant operation. Moreover, the resonant inductor from the converter topology T2 is sharing the energy, during the resonant cycle, with the capacitor  $C_R$ , making the overall losses of the resonant circuit larger for the T1 converter. However, the resonant inductor losses are not included in Figure 5.14 due to the more complicated HF inductor simulation model. Still the conduction and switching losses estimation results indicates a clear advantage for the topology T2. Therefore, this topology is chosen further.

### 5.2.2 Design of resonant passive elements and hardware layout

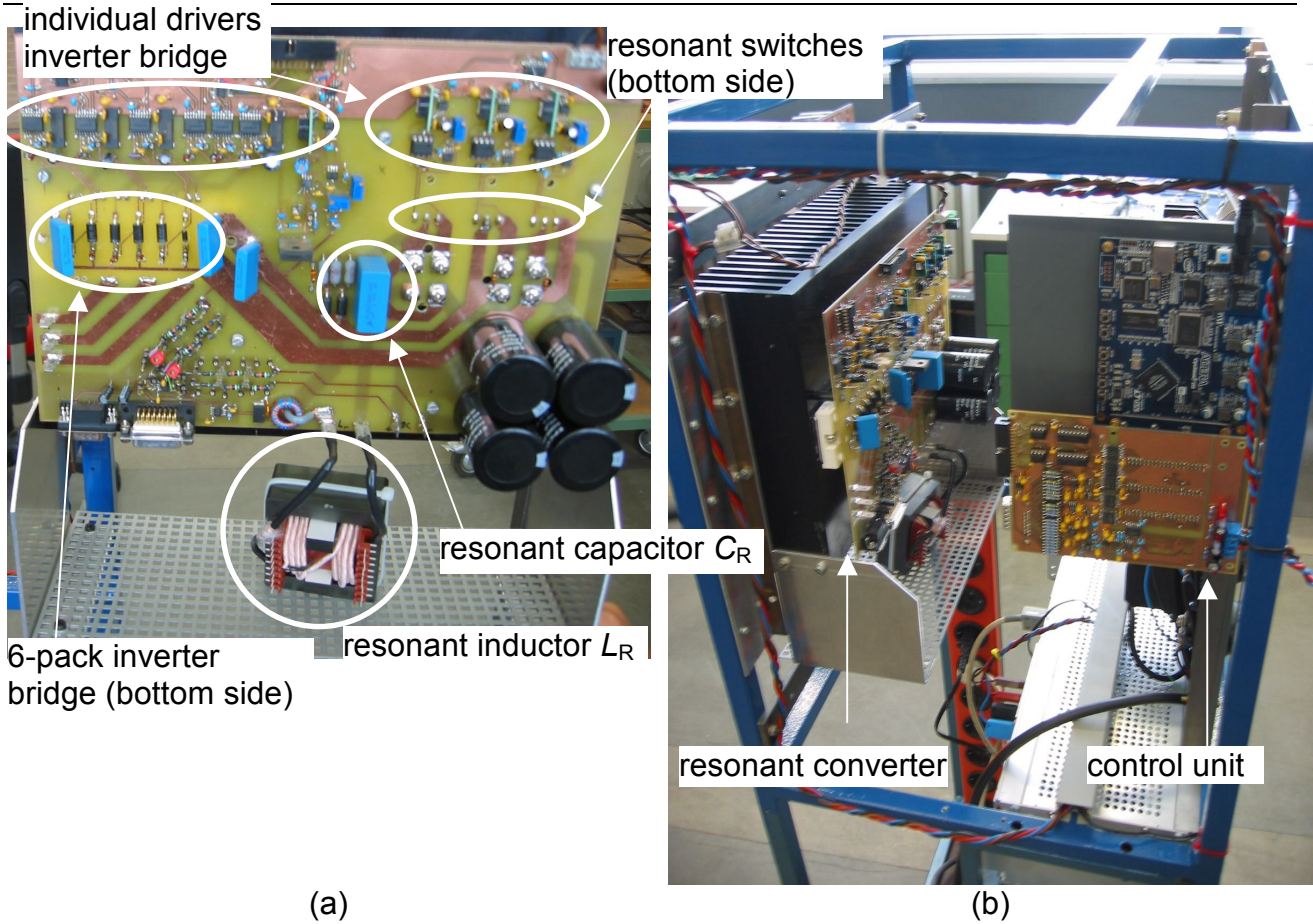
Following specifications to design the circuit parameters of the QR DC-link converter must be followed [72]:

- a) the inverter bridge voltage must be pulled down to zero during the resonant operation (ZVS) and again boosted to the DC-link voltage;
- b) the trip currents should be as small as possible in order to reduce the resonant circuit losses;
- c) it is also important to minimize the peak values of the resonant voltage and current in order to reduce losses and stress on the circuit devices;
- d) rising and falling slope of the inverter output voltage must be small for long cable drives, to avoid the voltage reflections at the motor terminals;
- e) the resonant transition interval must be designed to be much shorter than the switching time period of the inverter.

From all the mentioned specifications, a) is the most important condition for the soft switching of the inverter. Second b) and third c) specifications are satisfied with the calculation of the minimum trip currents  $I_{Tp1}$  and  $I_{Tp2}$ , see Figure 5.7. However, it is not possible to satisfy all other design objectives simultaneously. Therefore, a compromise between the resonant circuit parameters (namely between the motor-friendliness and efficiency characteristics of the QR converter) should be found to determine the value of the resonant elements for an imposed voltage slope  $dV/dt$ , because [72]:

- 1) The value of the resonant inductor  $L_R$  should be small so that the resonant transition interval and peak resonant capacitor voltage are small. However, a small  $L_R$  value could result in large peak resonant current and high  $dV/dt$ ;
- 2) An increase in the capacitor  $C_R$  value can limit the peak voltage of the resonant capacitor at the cost of high peak resonant current and  $dV/dt$ ;
- 3) The increase of the capacitor  $C_S$  value results in low  $dV/dt$  but high peak resonant current and resonant capacitor voltage.





**Figure 5.15: Resonant-converter board (a) and complete converter system with control part (b)**

The proper value of the resonant components can be obtained using the computer simulations. Because the optimisation of the QR converter topology is not the subject of this work, more details regarding the choice of the optimal parameter values, together with the variation characteristics of the parameters from simulations, can be found in [72]. Following values for the parameters of the resonant circuit lead to the best compromise in case of converter topology T2 (with the 34 m long LAPP cable connected between motor and inverter):  $(dV/dt)_{\min} = 600 \text{ V}/\mu\text{s}$ ,  $L_R = 30 \mu\text{H}$ ;  $C_R = 0.44 \mu\text{F}$ ;  $C_S = 0.147 \mu\text{F}$ .

Special attention was given to the inductor design, using the following principles:

- a magnetic core should be used to avoid the interference with the nearby electronic;
- a magnetic core with a high current-linkage is necessary to avoid the inductor saturation (the resonant peak currents can reach max 70A for  $I_{\text{Load}} = 22\text{A}$ );
- a HF inductor wire should be used to avoid the skin effect.

Thus, a specific core material and its dimensions were selected for the minimum losses, obtaining the following characteristics: value  $L_R = 30 \mu\text{H}$ , magnetic core: E71/33/32 (3F3 ferrite core type), HF copper wire area  $10 \text{ mm}^2$ .

The realized QR DC-link converter is shown in Figure 5.15 (a). A particular aspect regarding the operation of the resonant converter represents the operation mode M3. The shoot-through switching state of the inverter bridge is used in this case to assure a freewheel path for the resonant current. This state cannot be implemented with standard 6-pack or dual IGBT drive circuit with interlocking. Therefore, individual drivers have been chosen. The potential separation is realized with DC-DC converters, see Figure 5.15 (a). The similar considerations are valid also for the resonant switches, as they have to be controlled totally independent and potential-free. The resonant inductor can be observed on the lower part of Figure 5.15 (a). Figure 5.15 (b) shows the entire system, i.e. the resonant converter mounted in a rack, having the control unit nearby which will be detailed in the next section. The resonant inductor is mounted externally and connected to the

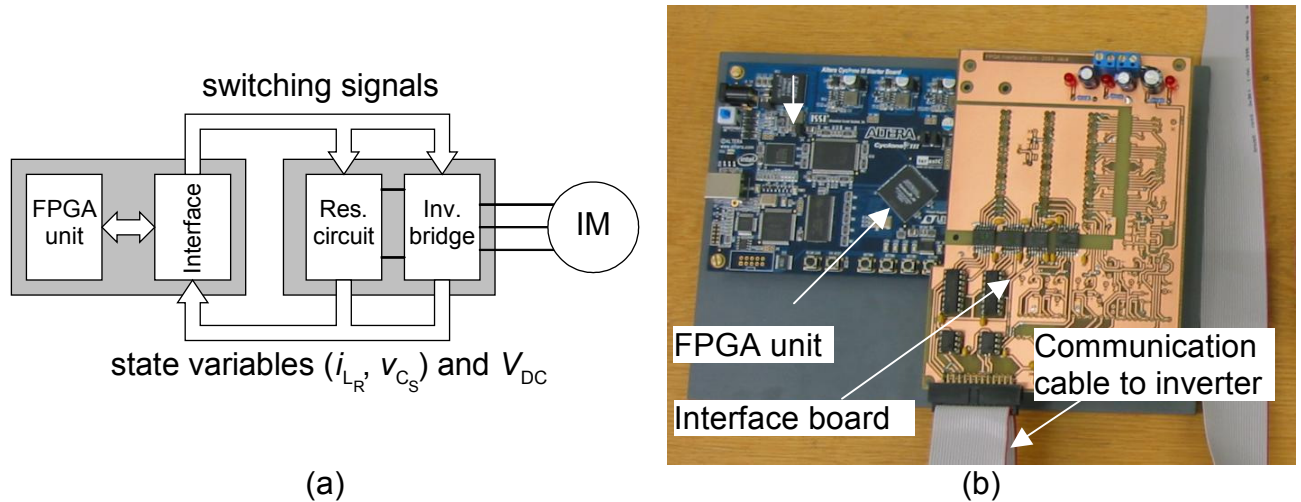


Figure 5.16: Control scheme (a) and control unit for the QR converter (b)

board. Thus, different prototypes for inductors can be tested regarding their efficiency. Also the snubber capacitors  $C'_S$  parallel to the switches were replaced by a single snubber capacitor  $C_S$  from Figure 5.2 (a). The needed ratio is  $C_S = 3 \cdot C'_S$ .

### 5.2.3 Control of QR DC-link inverter

Because the control implementation was the task of Mrs. Kedariseti, only a brief presentation of the system architecture is given. Due to the short resonant cycle and fast control decisions involved, a FPGA implementation is preferred to a DSP one. One resonant cycle takes minimum  $15 \mu s$ , a time interval in which the trip current must be compared with its reference. The off-line calculated levels of the trip current,  $I_{Tp1}$  and  $I_{Tp2}$ , are stored in a look-up table and are recalled depending upon the DC-link currents ( $I_O$  and  $I_{OX}$ ). In the same time interval, the switching signals for the three resonant switches and six inverter switches must be sent to the drivers. Also, special attention must be paid when choosing the size of the FPGA unit, because:

- it must contain sufficient logic cells to implement complex operations
- and include the control of both resonant cycle and induction motor.

Therefore, a FPGA unit from Altera®, from the Cyclon III® family with 25k cells, was chosen [72]. It is included in a development board with additional memory blocks of SSRAM (1MB) and DDR SDRAM (32MB). These memory blocks are used to store the look-up-tables for the trip currents. The Altera® software Quartus® is used for programming the board using the USB interface.

The communication between the FPGA and the transistor drivers must be realized with help of an interface. The main tasks of this interface are:

- acquisition of the state variables: resonant current, DC-link voltage  $V_{DC}$  and snubber-capacitor voltage for the resonant control;
- acquisition of the load currents for the control of both resonant cycle and motor;
- comparison of the resonant current with the trip-current values from the look-up tables;
- transmission of the switching signals from the modulator output of FPGA to the gate drivers; over-current protection during the resonant cycle.

Because the decisions during the resonant cycle must be very fast, the resonant current and snubber-capacitor voltage are compared with their reference values. The results are sent to the FPGA unit, which modifies correspondingly the switching state of the necessary switches. Only the load currents are digitalized and sent to the FPGA unit for motor control and protection purposes. The control scheme is shown In Figure 5.16 (a) together with the information flow between inverter and control unit. Figure 5.16 (b) illustrates more detailed the realized control unit with the FPGA unit and interface board.

### 5.3 Measurements and evaluation

Finally, the implemented QR converter was tested driving a Siemens 4 kW induction motor. The previous BBC 5-kW induction motor proved to be more difficult to drive due to the increased magnetization current (high-speed induction motor). The identification steps for data and parameters of the Siemens 4-kW induction motor are found in Appendix, subchapter 7.2.

A simulation model for the QR DC-link converter has been developed and implemented in Simplorer® network simulation software. Thus, it is possible to connect the developed simulation models for motor and cable in time domain to analyze the voltage overshoot at the motor terminals or the level of the CM voltage. Using the simulation models, the effects of voltage slope at the inverter output and reduction of the CM voltage can be studied.

#### 5.3.1 Resonant cycle

In Figure 5.17 the simulated (a) and the measured (b) waveforms of the state variables from the resonant circuit are shown. The PWM state of the inverter bridge changes when the snubber capacitor voltage is zero. For the selected parameters of the resonant circuit,

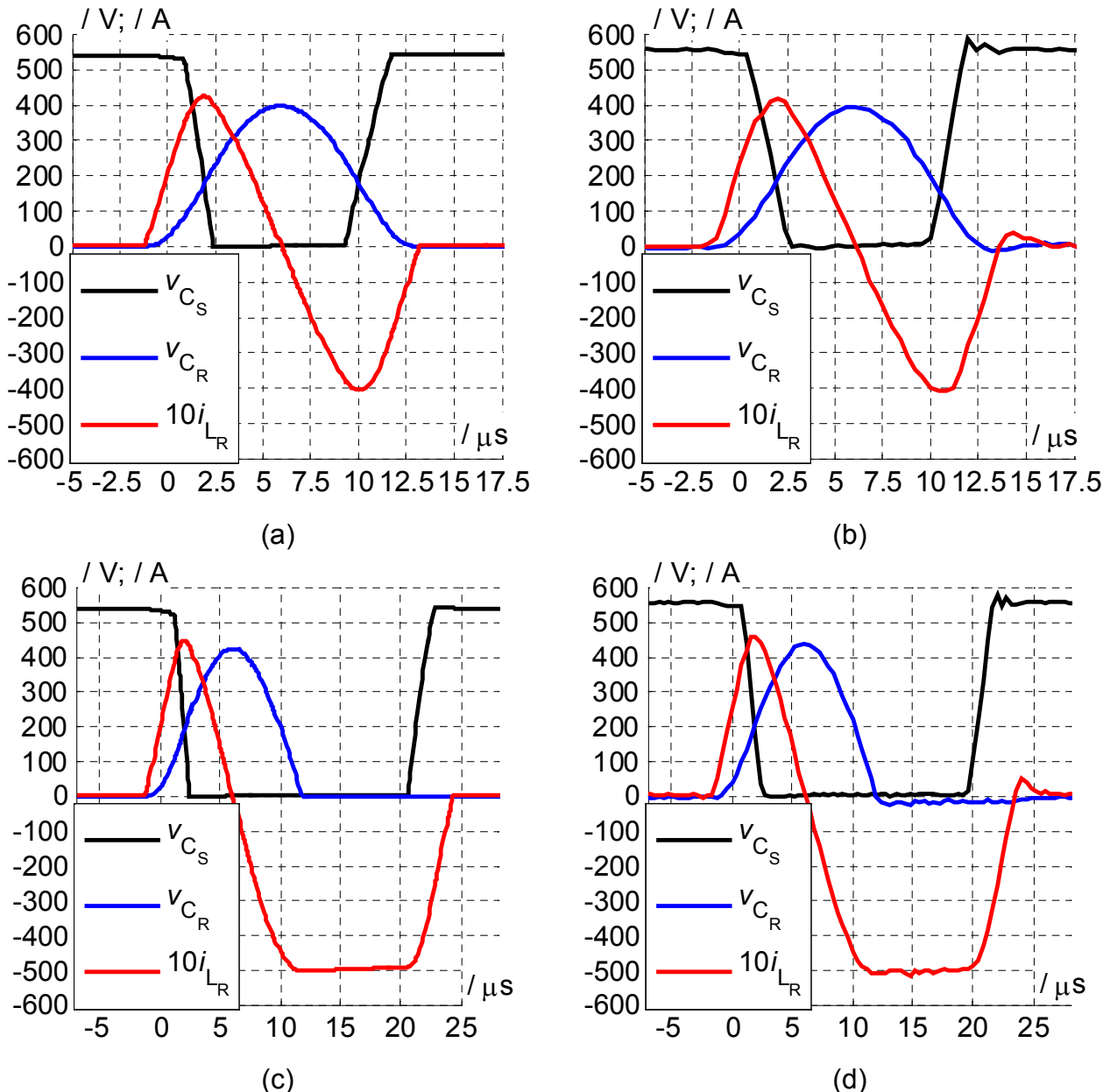


Figure 5.17: Simulated (a)+(c) and measured (b)+(d) state variables of resonant cycle



the peak resonant capacitor voltage will be always less than the DC-link level  $V_{DC}$ . Even though the peak currents in the resonant inductor are higher than the load current, the average value of the resonant current is low.

Because the zero-vector PWM state is implemented during the resonant cycle, using the modified PWM modulation technique from Figure 5.12 (b), the resonant operation has to be adapted for different modulation indexes, i.e. for lower fundamental frequencies it must be longer while for higher fundamental frequencies it must be shorter. This is achieved by delaying the operation mode M3 when the turn off of the equivalent switch  $S_{INV}$  is postponed (i.e. the next PWM state of the inverter bridge is postponed and the shoot-through state is kept, see Figure 5.2) [68], [70]. Of course, the level of the first trip current must be increased to allow more energy storage in the resonant inductor, necessary to complete the prolonged resonant cycle. Another disadvantage appears at the freewheel diode  $D_{R1}$ . Because the resonant capacitor  $C_R$  is already discharged, during the time interval where the resonant current is almost constant and negative, the diode  $D_{R1}$  is conducting. Thus, this diode has considerable conduction losses and special attention must be taken especially when driving the motor at full load.

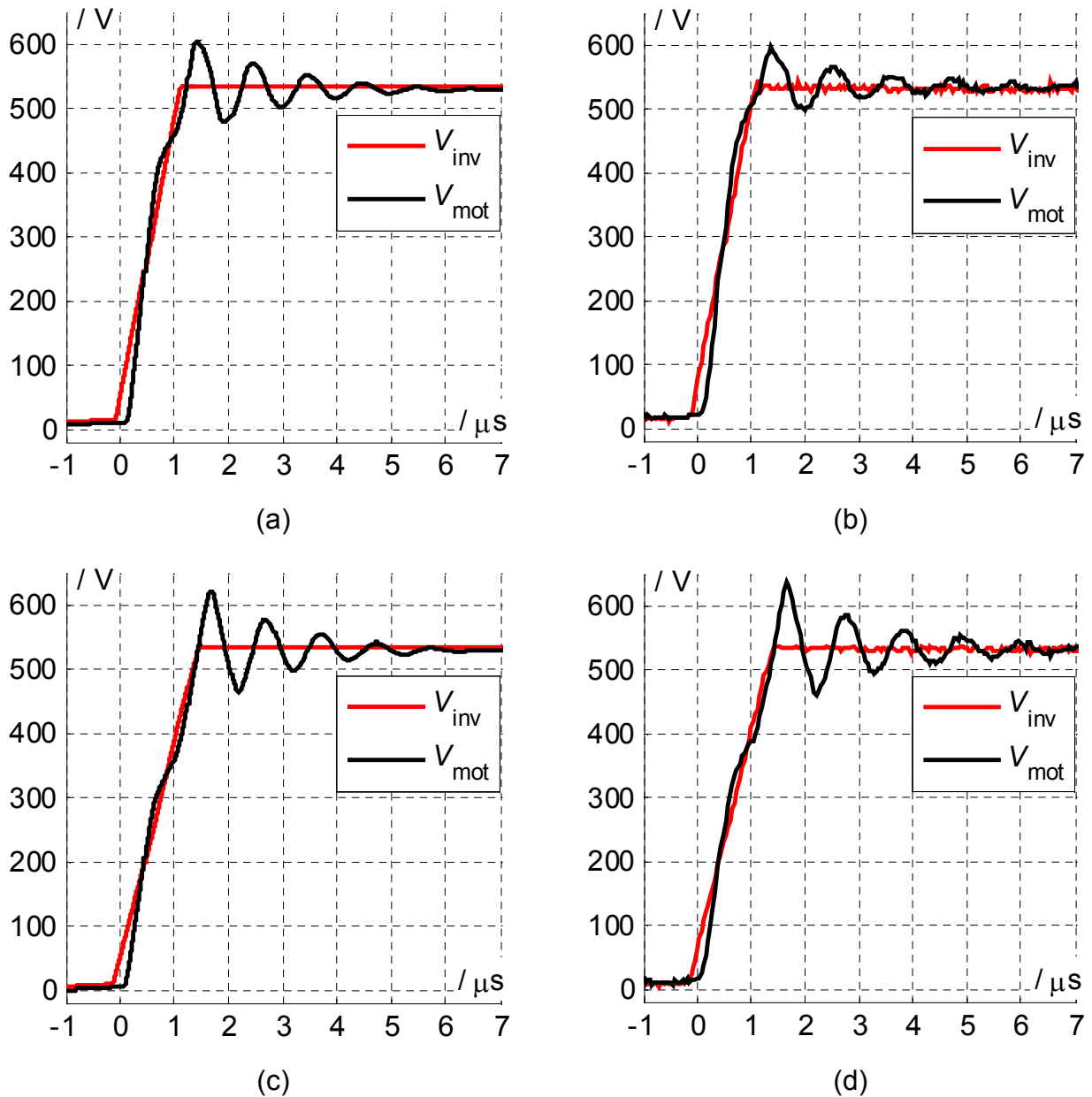


Figure 5.18: Simulated (a)+(c) and measured (b)+(d) line-line voltage at inverter and motor terminals

Such an extended resonant cycle is shown in Figure 5.17: (c) simulated and (d) measured. Under real conditions, the resonant current is slowly decreasing due to the losses in the resonant inductor. Therefore, the first trip current level  $I_{Tp1}$  has to be slightly increased to compensate these losses. Comparing the first case (short resonant cycle in Figure 5.17 (a)+(b)) with the second case (long resonant cycle in Figure 5.17 (c)+(d)), larger resonant peak currents are observed, necessary for the longer resonant operation (zero-voltage phase). The zero-voltage periods with different lengths are observed when the inverter bridge voltage drops to zero. Finally, the good agreement between the measurements and simulations leads to a good estimation of the parasitic effects.

### 5.3.2 Voltage reflections at motor terminals

Connecting the HF simulation models of the 34 m long LAPP cable and the Siemens motor (parameters from subchapter 7.2 for the motor model) to the QR inverter model, the motor terminals overvoltage is simulated. Thus, the simulation results, presented in Figure 5.18 (a), show the effect of the voltage gradient reduction on the line-line voltage. Here, the worst case was considered: the load current  $I_O$  has its maximum positive value, specific for the 4 kW selected point of operation, and the energy stored in  $C_S$  snubber capacitance is quickly removed, producing the fastest change in the inverter-voltage for the designed converter. The resonant elements were designed for the worst case, i.e. the voltage slope approximately 600V/ $\mu$ s and the overvoltage at the motor terminals under 20%. Measurements were conducted for the same operation conditions and the obtained results are plotted in Figure 5.18. The exact voltage slope at the inverter output and the overshoot percentage at the motor terminals are listed in Table 5.3. A good agreement between measurements and simulations is noticed.

Second, the motor current is small at no-load operation (only the magnetizing current is used to generate the motor flux) and the stored resonant energy during the resonant cycle is low. Therefore, the snubber capacitance  $C_S$  will no longer be quickly discharged as in the previous case. Simulations and measurements are shown in Figure 5.18 (c) and (d), respectively. The determined voltage slope and overshoot are presented also in Table 5.3. Although a smaller inverter voltage output slope is observed in this case, the voltage overshoot remains in the same range as in the previous case (full motor load) due to the small difference in the voltage slopes. Still, the worst case remains the full load operation where harmless overvoltage at the motor terminals is observed.

**Table 5.3: Inverter output voltage slope and voltage reflection overshoot under resonant operation**

	Inverter output voltage slope / V/ $\mu$ s		Voltage overshoot / %	
	simulated	measured	simulated	measured
Motor full load operation	433	430	13.2	12.1
No motor load operation	337	344	16.3	19.5

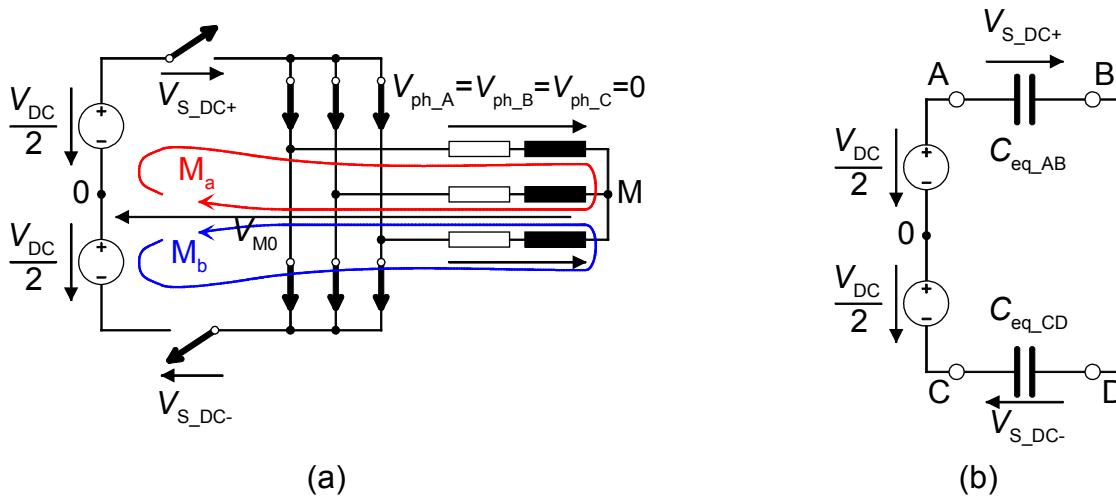
### 5.3.3 Common-mode voltage

As already presented in section 5.1.4, additional switches are used to entirely separate the DC link from the inverter bridge. Thus, the level of the common-mode voltage is reduced from  $V_{DC}/2$  to  $V_{DC}/6$ , which further determines the reduction of electrostatic discharge (EDM) bearing currents [16].

To analyze the reduction effect of the CM voltage, the simplified equivalent circuit from Figure 5.19 (a) is considered. During the resonant cycle, the inverter bridge is short circuited in the shoot-through state. This state is used as a zero-vector inside PWM, determining following relation for the phase voltages:

$$V_{ph\_A} = V_{ph\_B} = V_{ph\_C} = 0.$$

**Eq. 5.17**



**Figure 5.19: Simplified circuit for  $V_{S\_DC+}$  and  $V_{S\_DC-}$  calculation (a); equivalent capacitances circuit (b)**

The CM voltage is considered between the motor neutral point and the DC-link middle point [2]. Applying the rule of KVL for meshes  $M_a$  and  $M_b$ , the DC-link switches voltages are found to be:

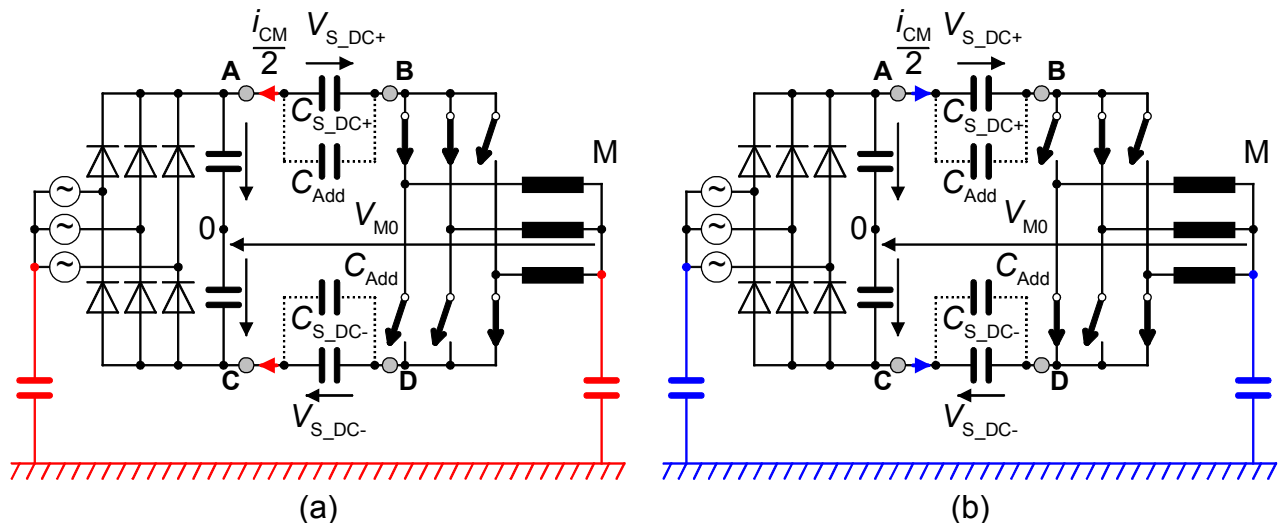
$$V_{S\_DC+} = V_{DC}/2 - V_{M0} + V_{ph\_A}, \quad \text{Eq. 5.18}$$

$$V_{S\_DC-} = V_{DC}/2 + V_{M0} + V_{ph\_C}. \quad \text{Eq. 5.19}$$

Imposing the condition  $V_{M0} = 0$  and inserting Eq. 5.17 in Eq. 5.18 and Eq. 5.19, the voltage expression for the DC-link switches is:

$$V_{S\_DC+} = V_{S\_DC-} = V_{DC}/2. \quad \text{Eq. 5.20}$$

Yet, measurements at the real setup show that both switches do not share the equal voltage. This happens due to the CM current flow, which is charging or discharging the equivalent capacitance seen from the CM voltage point of view. The flow of the CM current has the same direction through both positive (P) and negative (N) DC-link rails; see Figure 5.20. Moreover, the MOSFETs have a stray capacitance between drain and source in the turn-off state. Connected in parallel to the other stray capacitances to ground of the entire system, they build equivalent capacitances between drain and source connection of each DC-link switch (points pairs A and B, C and D respectively). These capacitances  $C_{eq\_AB}$  and  $C_{eq\_CD}$ , shown in Figure 5.19 (b), are connected in series during the resonant cycle (shoot-through inverter state) and have different values depending on the previous and next PWM switching states. Following situations, regarding  $V_{S\_DC+}$  and  $V_{S\_DC-}$  levels during



**Figure 5.20: CM current flow at  $V_{M0}$  decay (a); CM current flow at  $V_{M0}$  raise**

the resonant cycle, were found:

**Case 1)** when the resonant cycle follows a positive  $V_{M0}$  voltage (e.g. the previous PWM active state is 110 (1 – upper switch is closed and 0 – lower switch is closed), shown in Figure 5.20 (a)), the voltage  $V_{S\_DC+}$  is lower than  $V_{S\_DC-}$ :

$$V_{S\_DC+} \approx V_{DC} / 3; V_{S\_DC-} \approx 2 \cdot V_{DC} / 3.$$

Eq. 5.21

From Figure 5.19 (b), following relation for the equivalent capacitances is obtained:

$$C_{eq\_AB} \approx 2 \cdot C_{eq\_CD}.$$

Eq. 5.22

Inserting Eq. 5.21 and Eq. 5.17 in Eq. 5.18 and Eq. 5.19,  $V_{M0}$  is obtained:

$$V_{M0} \approx V_{DC} / 6,$$

Eq. 5.23

i.e. the CM voltage remains almost unchanged during the resonant cycle. The corresponding measurements are shown in Figure 5.21 (a) for RL passive load.

**Case 2)** when resonant cycle follows a negative  $V_{M0}$  voltage (e.g. previous PWM active state is 010, see Figure 5.20 (b)), the voltage  $V_{S\_DC+}$  is higher than  $V_{S\_DC-}$ , namely:

$$V_{S\_DC+} \approx 2 \cdot V_{DC} / 3; V_{S\_DC-} \approx V_{DC} / 3.$$

Eq. 5.24

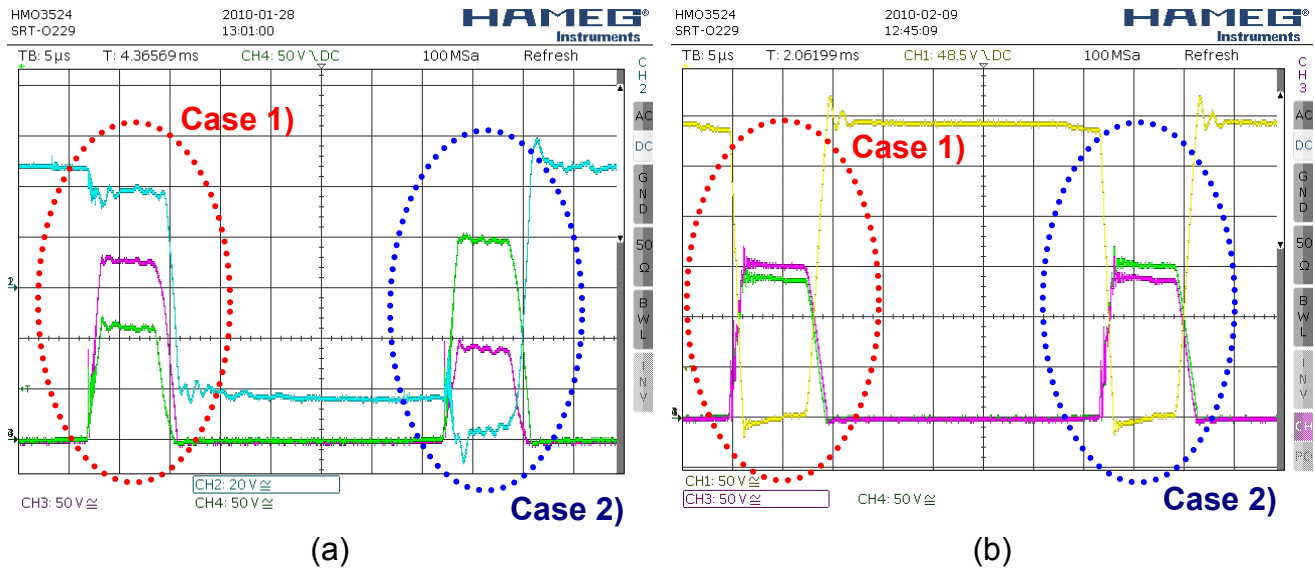


Figure 5.21: Unequal voltage sharing (RL-passive load connection): no  $C_{Add}$  (a);  $C_{Add} = 15$  nF (b)

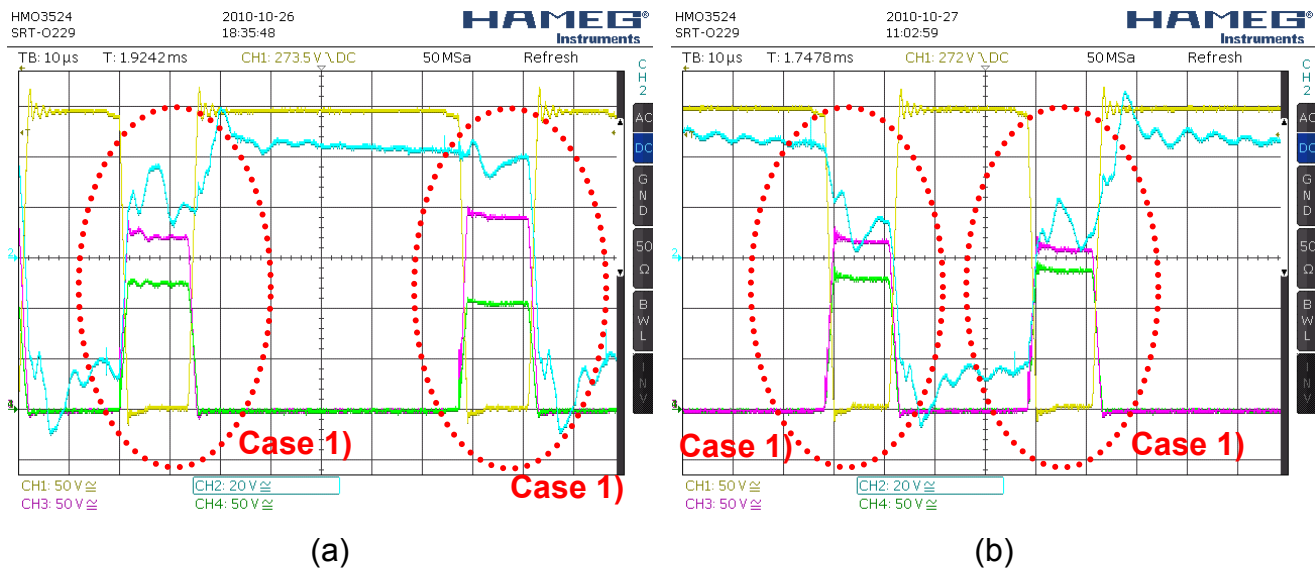


Figure 5.22: Unequal voltage sharing (Motor load connection):  $C_{Add} = 22$  nF (a);  $C_{Add} = 37$  nF (b)

**Legend:** inverter bridge voltage  $V_{C\_S}$  (yellow) – 50V/div; CM voltage  $V_{CM}$  (blue) – 20V/div;  $S\_DC+$  voltage (green) – 50V/div;  $S\_DC-$  voltage (magenta) – 50V/div; time – 5(10) $\mu$ s/div

From Figure 5.19 (b), following relation for the equivalent capacitances is obtained:

$$C_{eq\_AB} \approx C_{eq\_CD} / 2.$$

Eq. 5.25

Inserting Eq. 5.24 and Eq. 5.17 in Eq. 5.18 and Eq. 5.19,  $V_{M0}$  is obtained:

$$V_{M0} \approx -V_{DC} / 6,$$

Eq. 5.26

i.e. the CM voltage remains almost unchanged during the resonant cycle. The corresponding measurements are shown in Figure 5.21 (a) for the RL-passive load.

Thus, it is noticed that the unequal voltage over the DC-link switches alternates dependent on the active PWM state, previous to the resonant cycle. To compensate this effect, additional capacitances  $C_{Add}$  are connected in parallel to each DC-link switch, i.e. to increase  $C_{eq\_AB}$  and  $C_{eq\_CD}$ . Following conditions are therefore necessary:  $C_{Add} \gg C_{eq\_AB}$  and  $C_{Add} \gg C_{eq\_CD}$ . The increase of the parallel capacitances to  $S_{DC+}$  and  $S_{DC-}$  is possible because these switches turn on and off under ZVS conditions. However, too large values for  $C_{Add}$  are not optimal due to an increase of the oscillations in  $V_{S\_DC+}$  and  $V_{S\_DC-}$  transients, which finally lead to an increase of the oscillations in the inverter output voltage. An optimal value of  $C_{Add} = 15$  nF was empirically found for the considered system: inverter-cable-RL passive load. The measurement results using the parallel capacitors  $C_{Add}$ , are shown in Figure 5.21 (b) for both **Case 1)** and **Case 2)**.

A major role in  $C_{eq\_AB}$  and  $C_{eq\_CD}$  capacitances play the ground stray capacitances of the cable and motor. When the RL passive load is used, only the stray capacitance of the cable to earth is accounted. When connecting the motor,  $C_{eq\_AB}$  and  $C_{eq\_CD}$  are much larger due to the stray capacitance of the motor to ground. Thus, a value of  $C_{Add} = 15$  nF is no longer satisfying the condition  $C_{Add} \gg C_{eq\_AB(CD)}$ . The measurements show that even  $C_{Add} = 22$  nF is not sufficient, see Figure 5.22 (a). Only a value of  $C_{Add} = 37$  nF leads to visible improvement of the voltage sharing across the DC-link switches, see Figure 5.22 (b). The connected motor determines a change in the CM system. Thus, only one case mentioned before will be dominant, namely **Case 1)**, see Figure 5.22.

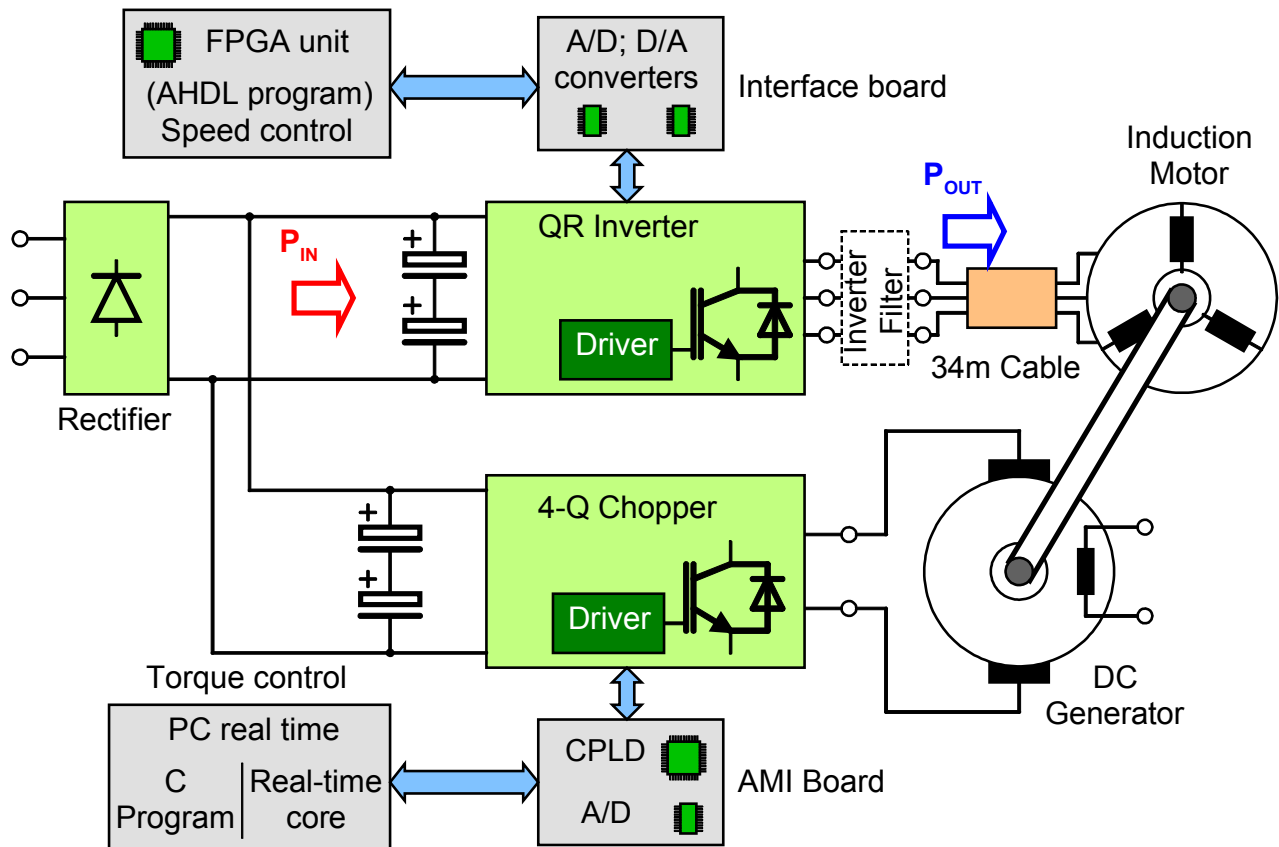


Figure 5.23: Induction motor – DC generator system for efficiency measurements



### 5.3.4 Induction Motor – DC Generator system for efficiency measurements

In order to measure the inverter efficiency, the system inverter–long cable–induction motor (IM) was extended with a DC generator (DCG), connected mechanically to the shaft of the IM and driven by a H-bridge converter (4-Quadrant Chopper). The DC-link circuits of QR converter and the H-bridge converter are connected together to recover a part of the energy used to drive the IM.

Figure 5.23 shows the schematic of the IM-DCG system. The QR inverter is controlled by the FPGA unit and can drive the IM in the hard-switching (HS) or the soft-switching (SS) modes. During the HS mode, the switches for the DC-link separation remain always turned-on and the resonant switch  $S_R$  turned-off. Only when the SS operation is needed, this switch is used. Between the QR inverter and IM the 34m-long, shielded LAPP cable is used. Additionally, when the inverter is operated in the HS mode, different inverter output filters are used to reduce the parasitic effects, namely the  $dV/dt$  filter (reduces only the slope of the inverter output voltage) Schaffner FN510 [82] and the Sine-Wave EMC filter (with DC-link clamping to filtering the line-earth voltage) Schaffner FN530 [83].

The DC machine is operated as a generator using the 4Q chopper. The energy recovered is not fed back to the mains but used further for driving the IM. This is realized connecting the DC-link circuits of both inverter and chopper together, see Figure 5.23. The 4Q chopper is controlled using a real-time PC and an AMI interface board, the same system being presented in section 3.1.3.

The speed of the IM is first kept constant using the Field-Oriented Control (FOC) method (implemented in FPGA by Mrs. Kedarisetti) and then a constant torque is applied to the DCG by maintaining a constant value for the armature current. Thus, a fixed operation point is used to measure the efficiency of the QR inverter. This is realized using a power meter (LMG 450) with four channels: one channel is used to measure the input power  $P_{IN}$  (DC side voltage and current) and the other three channels are used to measure the inverter output power  $P_{OUT}$  (three line-line voltages and phase currents). The ratio between  $P_{OUT}$  and  $P_{IN}$  represents the inverter efficiency  $\eta$ .

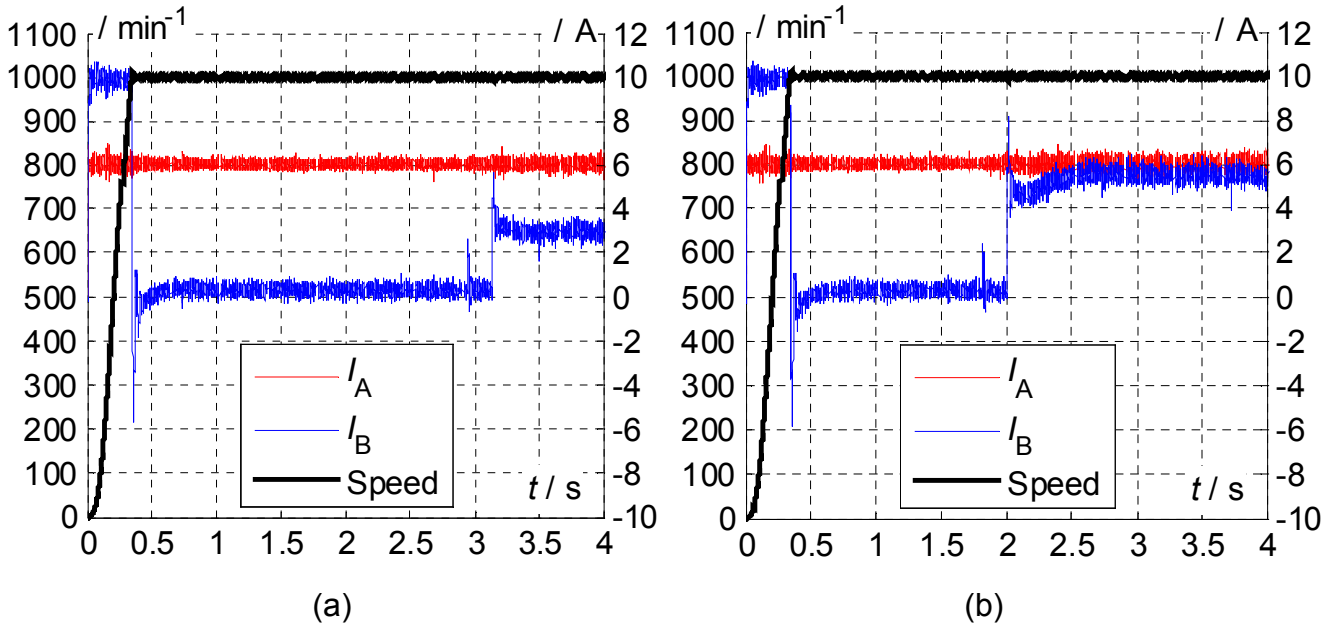


(a)



(b)

Figure 5.24: DC generator – induction motor system (a) and 4Q-chopper for DC machine braking (b)



**Figure 5.25: Measured speed, torque ( $I_B$ ) and flux ( $I_A$ ) producing current components for  $T_{\text{Load}} = 10 \text{ Nm}$  (a) and  $T_{\text{Load}} = 15 \text{ Nm}$  (b)**

Both electric machines are coupled mechanically, shown in Figure 5.24 (a). Figure 5.24 (b) illustrates the 4Q chopper used for the DC generator braking (bottom side) and the AMI interface board (topside) used to control the converter.

To exemplify the implementation of field oriented control (FOC) under resonant operation, induction motor measured speed and the two current components used for FOC [2], i.e.  $I_A$  used to produce the nominal flux and  $I_B$  used to produce the necessary torque to maintain the speed constant, are plotted in Figure 5.25. First, a load torque  $T_{\text{Load}} = 10 \text{ Nm}$ , maintained constant using the DC generator (armature current control with constant excitation flux), is applied at the time instant  $t \approx 3.15 \text{ s}$ , see Figure 5.25 (a). It can be noticed that the current component  $I_B$  is increasing to app. 3A to generate the necessary torque. The current is controlled using the “Amplitude Optimum” method [2]. During the period where no torque is applied,  $I_B$  is controlled to 0. At the beginning, the nominal torque is applied ( $I_B \approx 10 \text{ A}$ ) to accelerate the motor in less than 0.4 s from stand still to the constant speed  $1000 \text{ min}^{-1}$ . In a similar way, the results for  $T_{\text{Load}} = 15 \text{ Nm}$  are shown in Figure 5.25 (b). The load torque from DCG is applied in this case at the time instant  $t \approx 2 \text{ s}$ , see the step change in the current component  $I_B$  from 0 to app. 5.5 A.

### 5.3.5 Efficiency measurements and evaluations

In order to evaluate the effect of the inverter output filters and of the resonant operation, the measurements, regarding the inverter output and motor input line-line (line-earth) voltage, together with the CM voltage, were conducted for the following configurations:

1) *Inverter without output filter + LAPP cable + motor load*, see Figure 5.26. The line-line voltage waveform oscillations (a) are clearly visible at the motor terminals and their oscillation period depends exclusively on the cable stray elements. Similar oscillations are observed at the line-earth voltage (b), i.e. CM ground current occurs with high amplitudes. The CM voltage (c) presents, beside the harmonic specific to a space vector modulation (stepwise between  $-V_{\text{DC}}/2$  levels [2]), high harmonics due to long cable (high oscillations).

2) *Inverter with  $dV/dt$  output filter + LAPP cable + motor load*, see Figure 5.27. The effect of  $dV/dt$  filter is reflected in line-line voltage slope (a), which is lower in this case. Still there is a voltage overshoot at motor terminals and the voltage oscillations on the cable are influenced by the filter inductance and capacitance. Similar conclusion is valid for the line-earth voltage (b), i.e. the voltage slope is lower (smaller peaks for CM ground current).

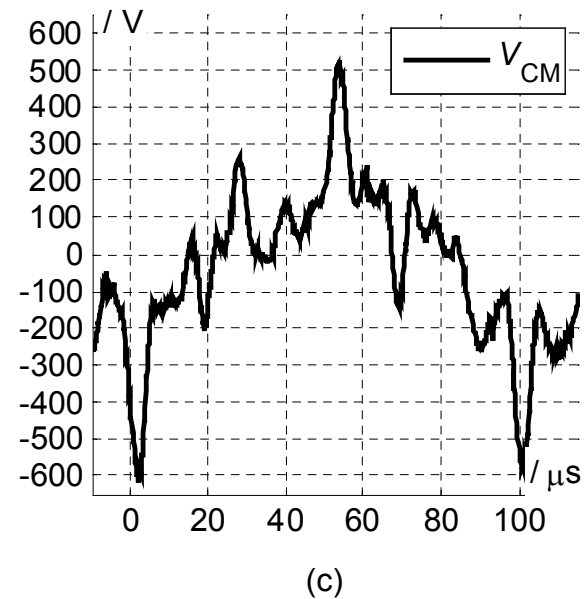
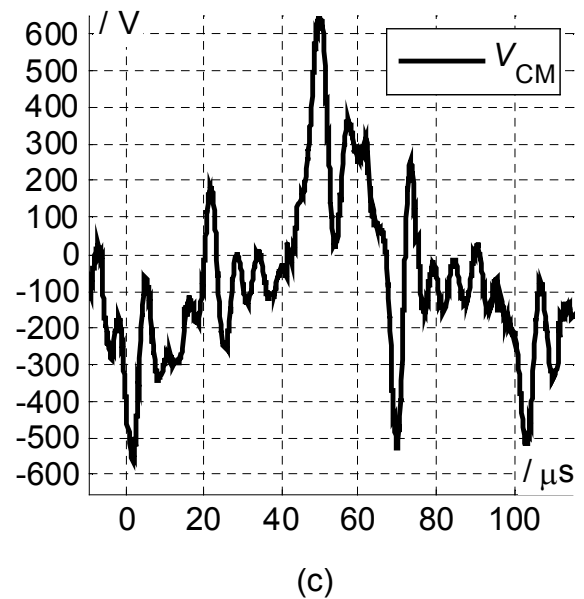
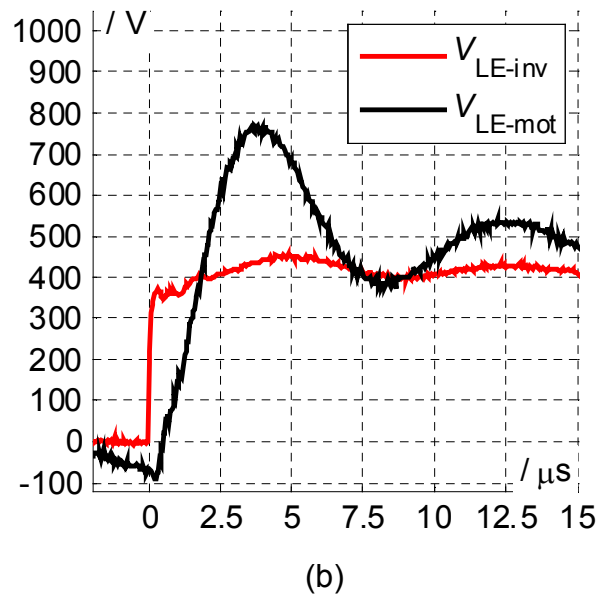
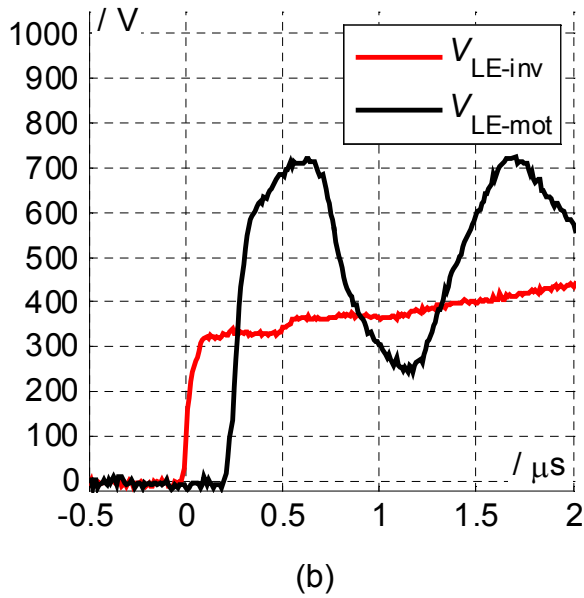
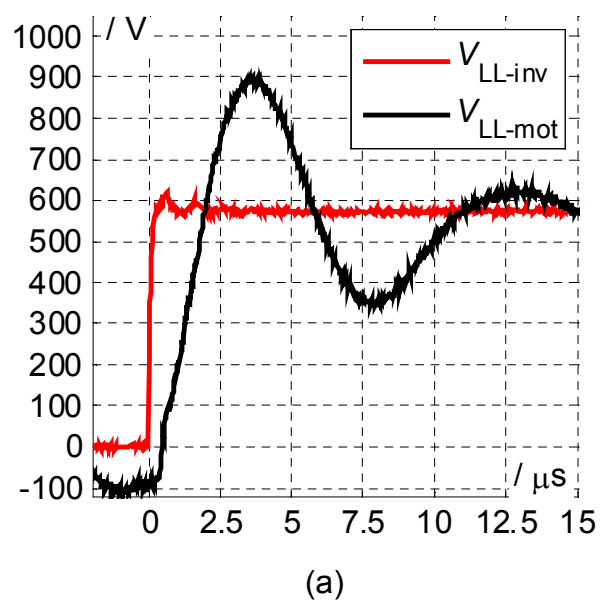
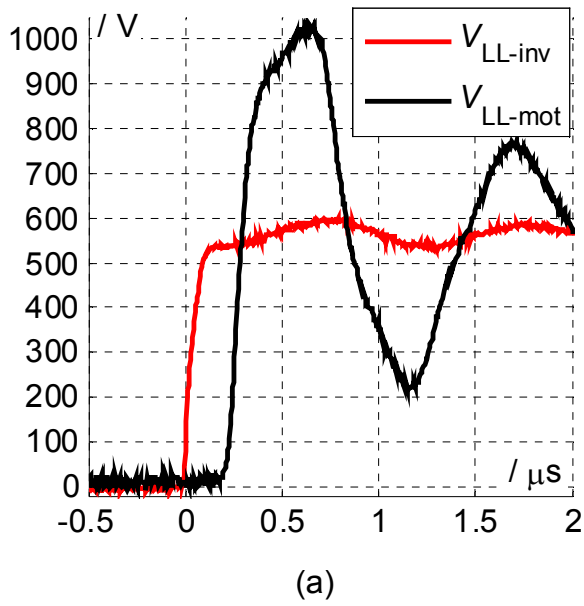
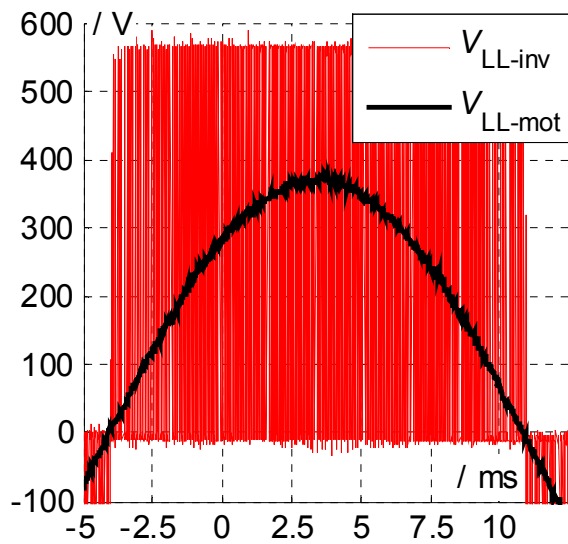


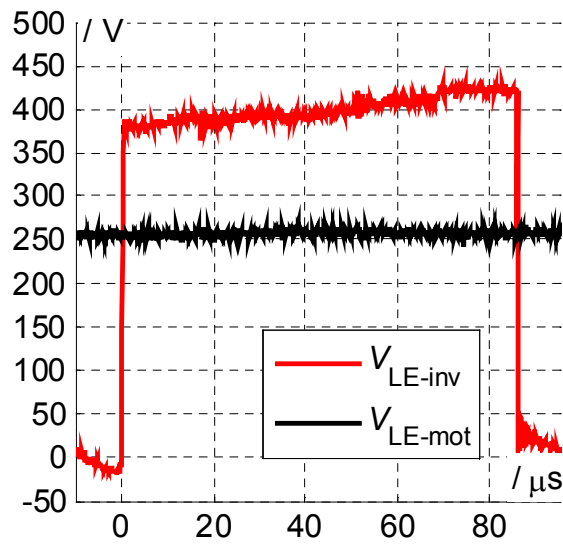
Figure 5.26: Results for Hard-Sw. + NO filter

Figure 5.27: Results for Hard-Sw. + dV/dt filter

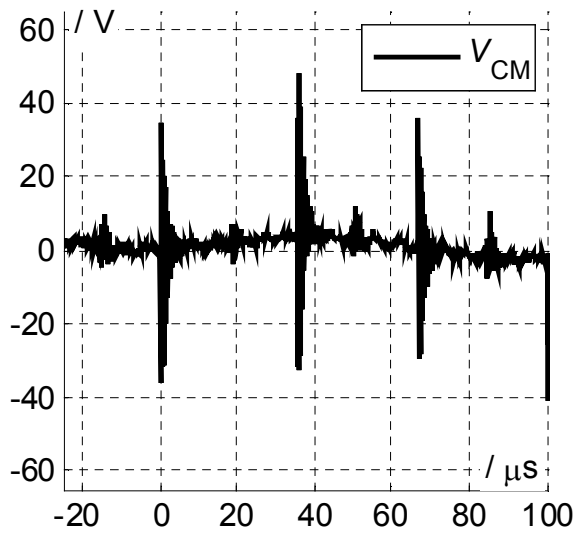




(a)

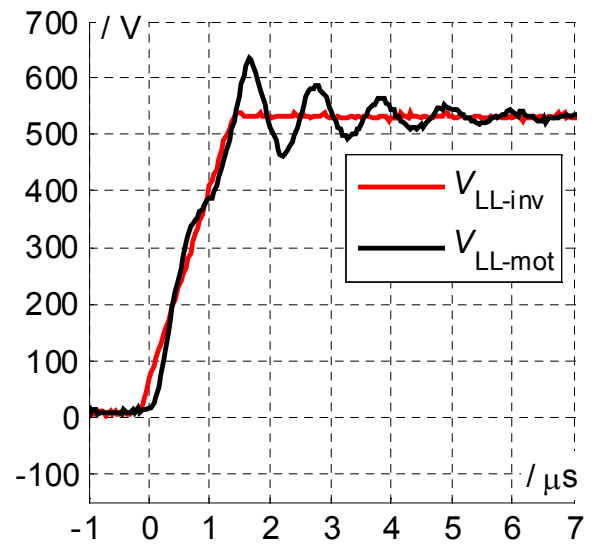


(b)

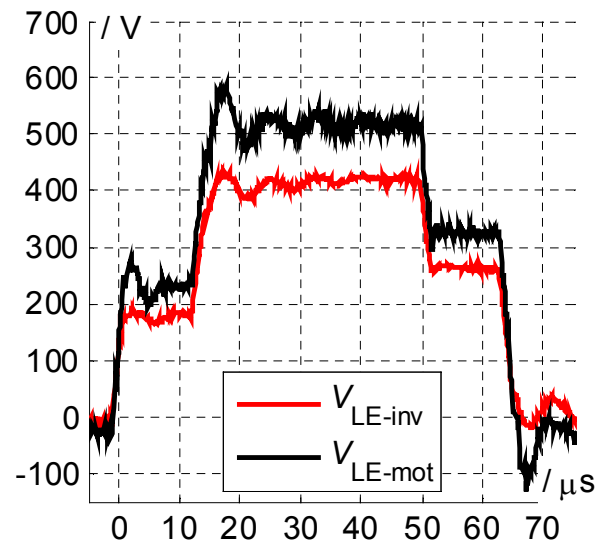


(c)

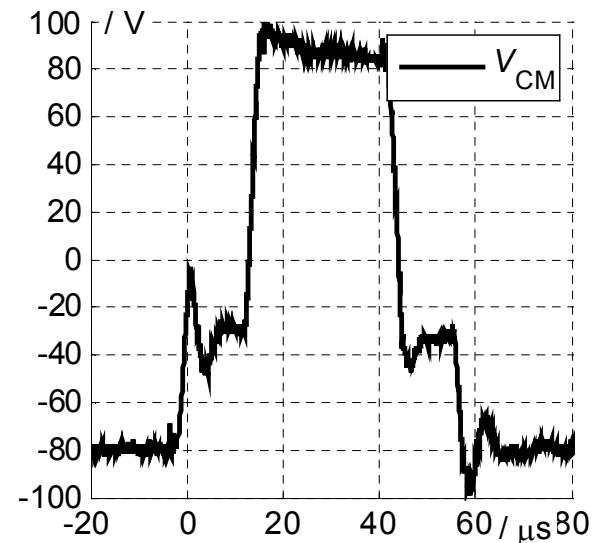
Figure 5.28: Hard-Sw. + Sine-Wave EMC filter



(a)



(b)



(c)

Figure 5.29: Results for resonant operation

The CM voltage has lower oscillations than in the previous case also with different frequency.

3) *Inverter with Sine-Wave EMC filter + LAPP cable + motor load*, see Figure 5.28. Because the cutoff frequency lays between switching and motor fundamental frequencies, the voltage at the filter output is transformed from a train of rectangular pulses into a sinusoidal wave (motor fundamental frequency), see (a) – half a fundamental period. Looking more in detail, the train of rectangular pulses is noticed at inverter side (line-earth voltage (b)), whereas the motor side line-earth voltage is almost constant for this time window. The CM voltage (c) is filtered almost completely (high capacitive coupling to earth). Much smaller oscillations (app.  $\pm 30$  V) occur during the PWM commutation.

4) *Inverter with resonant operation + LAPP cable + motor load*, see Figure 5.29. As already presented in section 5.3.2, the lower voltage slope at the inverter output leads to a reduction of the voltage overshoot at the motor terminals (a). The voltage slope depends directly on the resonant passive elements. Therefore, the prototype converter was designed to deliver a voltage slope at the inverter output of app.  $600 \text{ V}/\mu\text{s}$  for the worst

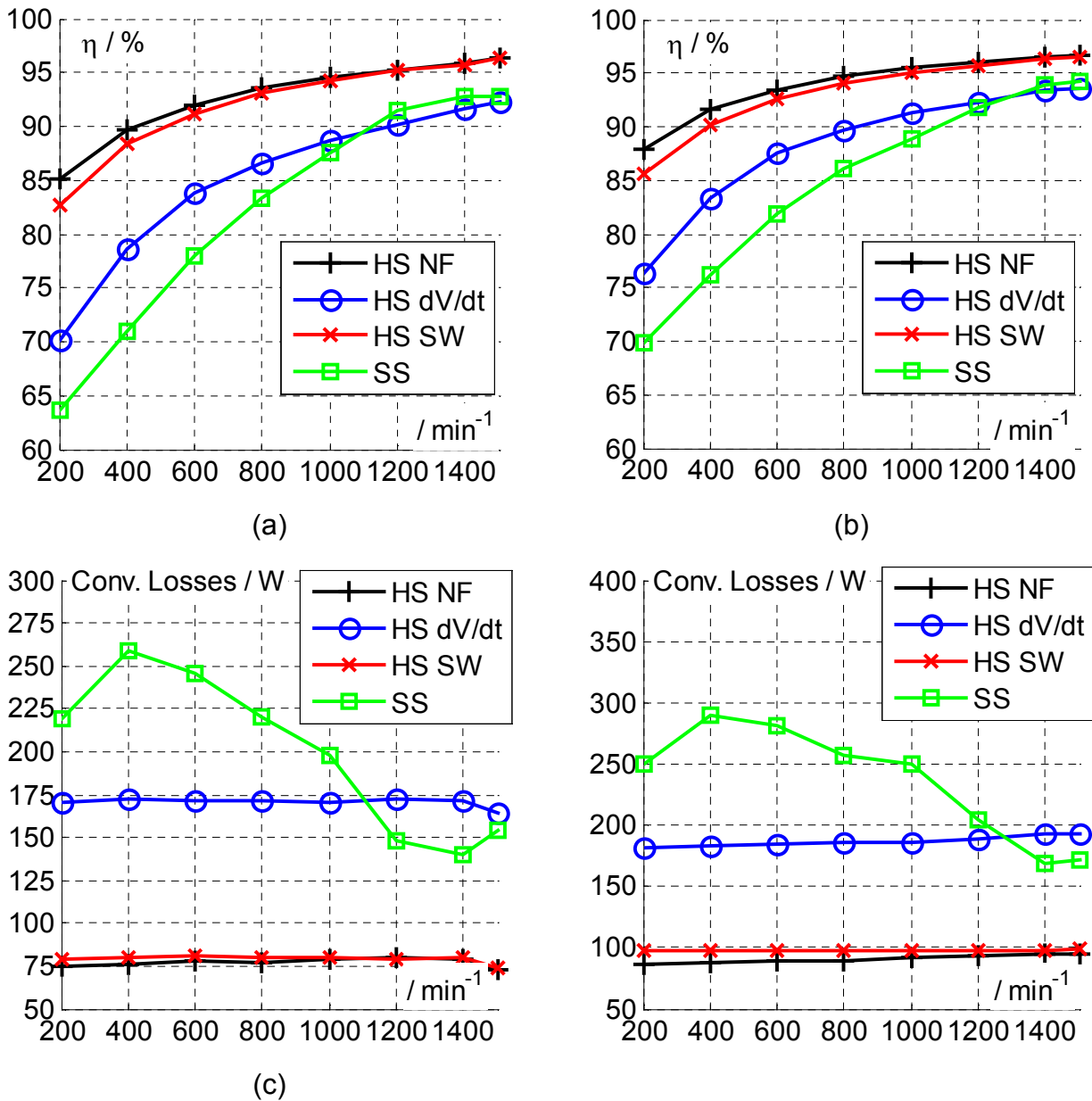


Figure 5.30: Measurements for efficiency at  $T_{\text{Load}} = 10 \text{ Nm}$  (a) and  $T_{\text{Load}} = 15 \text{ Nm}$  (b);  
Measurements for converter losses at  $T_{\text{Load}} = 10 \text{ Nm}$  (c) and  $T_{\text{Load}} = 15 \text{ Nm}$  (d)

case. This value is sufficient when cables up to 35 m are used. Due to the DSC-like modulation technique, used to implement the zero-vector period during the resonant cycle, and due to the complete DC-link separation during this period, the use of additional DC-link switches determines a similar waveform for the line-earth voltage (b) and CM voltage (c). Moreover, due to the small voltage slope, there are no line-earth voltage reflections at the motor side, i.e. small CM ground current peaks will occur. The CM voltage has the same stepwise waveform, as presented in section 5.3.3, alternating between  $\pm V_{DC}/6$  values during the active vector period and zero during the resonant cycle. As already shown, due to the parasitic capacitances to earth of the entire system, the voltage sharing between  $S_{DC+}$  and  $S_{DC-}$  switches is not equal. Only with auxiliary parallel capacitances the effect of the unequal voltage sharing is reduced, see section 5.3.3. Thus, the CM voltage level is not zero during the resonant cycle, but a relative small offset of approximately 20 V can be noticed, see Figure (c) where a 37 nF capacitance is connected parallel to  $S_{DC+/-}$ .

Finally, measurements for the efficiency and the losses of the converter were conducted at 4 drive configurations for two different load torques, see Figure 5.30:

- HS NF = hard-switched converter with no output filter;
- HS dV/dt = hard-switched converter with dV/dt-output filter;
- HS SW = hard-switched converter with SineWave EMC filter;
- SS = converter with resonant operation;

Lower efficiency can be noticed for the QR converter at low motor speeds due to the extended resonant operation, see Figure 5.17 (c) and (d). Here, more energy has to be saved in the resonant elements and therefore higher losses will occur. Yet, the efficiency of the QR converter is higher than the one of the dV/dt-filter configuration at higher motor speeds (high modulation index), because the resonant operation is short. This can be observed also from the measurements of the converter losses, see Figure 5.30 (c) and (d). While for dV/dt and SineWave EMC filters the losses remain relatively constant with an increased motor speed, the lower motor speeds determine higher losses for the resonant-operated converter. Only at high motor speeds, the resonant converter becomes competitive.

The selected SineWave EMC filter determines sinusoidal voltages and currents at the inverter output. Because the current will not oscillate at the inverter side, the losses in the inverter are reduced. But the filter itself produces losses due to the low cutoff frequency of the filter. Additional connections to the DC-link bus bars provide a feed-back path for the clamped energy to flow back to the DC link. Thus, the filter losses are reduced significantly. Having a part of the inverter losses shifted in the filter and the filter losses reduced with the DC-link feed-back, the total efficiency of the system inverter + SineWave EMC filter is almost similar to the efficiency of the system inverter + no output filter. This can be followed in Figure 5.30. The losses of the SineWave EMC filter were measured also separately, and found to correspond to the data-sheet description, i.e.  $P_{Loss} = 50$  W for the corresponding power class of app. 5 kW at the rated load current.

It must be mentioned that the measurements in Figure 5.30 are performed at a first QR converter prototype. There is an important improvement potential, regarding the losses, which can be further exploited. Following major directions may be followed:

- inductor losses can be improved, if better inductor cores are used. Another possibility is to use no magnetic cores. In this case there will be no core losses and the magnetic field will not be constraint inside the core. Therefore, special attention should be paid for the EMI emissions and increase of copper losses;
- better semiconductor devices, like SiC materials, may improve the overall efficiency;
- the modulation technique may be improved to avoid the resonant cycle to be extended excessively. Thus, a limit for the length of the resonant cycle can be adopted and the resonant operation started only when the motor speed exceeds a minimum value.

Concluding, the QR converters can be used in electric drives with long cables to reduce the parasitic effects. Using the proposed modifications, not only the voltage overshoot will be significantly reduced, but also the electrostatic EDM bearing currents, thanks to the significant reduction of the common-mode voltage  $V_{CM}$  levels. Therefore, important improvements are obtained regarding the motor-friendly characteristic. Regarding the energy-efficient characteristic, an active control of the resonant cycle leads to a better use of the energy storage during the resonant cycle. However, further improvements remain to be investigated, as the efficiency becomes competitive, compared to the “hard-switched converter + output filter”, only at high modulation index (high motor speeds).

## 6 Conclusions and outlook

Fast-switching semiconductor devices are nowadays implemented in electric drives with VSI to allow higher switching frequencies, which leads finally to a reduction of the harmonic content in electrical machine and decrease of losses. Also, faster switching transients determine lower switching losses, making the semiconductor devices more efficient. However, HF parasitic effects have been reported and associated to the use of the fast-switching semiconductors with long motor cables. Due to the impedance mismatch between the cable and stator windings, especially for low-power motors, the traveling wave along the cable reflects at the motor terminals [6] [10], resulting in a voltage peak of 2 times the DC-link level or, in certain conditions, even higher [5]. Moreover, repetitive bearing currents were observed, which lead eventually to the damage of the bearing.

The purpose of this work is first to model the main components of the electric drive, i.e. the inverter seen as the source of the traveling waves, the cable seen as the medium for the wave propagation and finally the motor at the cable end. The simulation models are detailed together with their parameterization methods and finally validated by comparison with measurements on a real setup.

Second, several methods for reducing the HF parasitic effects are investigated using the developed simulation models. Thus, the efficiency of the developed simulation models is demonstrated by comparing the conducted measurements with simulations for the same case.

**Table 6.1: Analysis and selection of HF simulation models for electric drives**

Simulation model type		
IGBT	Behavioral model	Physics-based model
	describes the semiconductor behavior using an equivalent circuit based on the stray elements of the semiconductor	describes the semiconductor with voltage and current sources, based on the physical equations of the semiconductor
Advantages/ Disadvantages	+ simple to parameterize from the data-sheet information and measurements at the IGBT terminals – does not describe all transient phenomena (e.g. the reverse-recovery effect of the anti-parallel diode)	+ describes the transient phenomena accurately using the carrier equations – needs the physical dimensions to be known (e.g. doping concentrations, epitaxial layer width, etc.)
Evaluation	was chosen due to the simple parameterization and simplicity	was found inappropriate due to the inaccessible physical semiconductor data
Cable	Transmission line model	Lumped parameter model
	the cable is considered as a transfer function of both time and space which connects the incident and reflected waves	also called “distributed parameters model” is based on the ladder connection of more individual $\Gamma$ equivalent circuits
Advantages/ Disadvantages	+ easy to implement and small simulation times – cannot include couplings between cable strings + HF skin and proximity effects	+ more accurate than transmission line model – is complex and the physical data is needed for the model parameterization
Evaluation	is not preferred due to the missing representation of the conductor couplings and losses; is optimal for frequency domain	was chosen due to the increased accuracy, simple parameter determination and time domain simulation
Motor	Behavioral model (equivalent circuit)	Physics-based model (distr. param.)
	Same as for IGBT, the model is based on the equivalent circuit parameterized from the measurements of the input impedance	based on the traveling wave theory, the motor windings are modeled by connecting more individual $\Gamma$ circuits
Advantages/ Disadvantages	+ easy to implement and to parameterize – does not include the voltage sharing effect at the first stator windings	+ more accurate than the behavioral model – is complex and physical data is needed for the parameterization of the model
Evaluation	was chosen because of the simplicity and satisfactory results	is difficult to implement due to the unknown physical structure of the motor

In the third part of this work, a quasi-resonant DC-link converter is analyzed and implemented for the reduction of the HF parasitic effects. Two important aspects are regarded individually: motor-friendly characteristic of the converter (concerning the reduction of the HF parasitic effects) and high-efficiency characteristic (concerning the losses reduction for this type of converters in order to make it competitive with other solutions, e.g. hard-switched inverter with output filter). Using the already-developed simulation models for cable and motor, the simulations, regarding the effect on the voltage overshoot and CM voltage, are presented together with the measurements at a real setup.

## 6.1 High-frequency simulation models

In order to investigate the HF-related phenomena in electric drives, a good and comfortable solution is the off-line method using simulation models. Therefore, reliable models for each part of the electric drive have to be developed. In chapter 2, the adopted simulation models are presented for inverter, cable and electric machine together with their parameterization methods. They are summarized again in Table 6.1. Finally, connecting the three simulation models together, the total electric drive model is obtained.

These simulation models are then validated by measurements at a real setup in chapter 3. Few small improvements are made to the IGBT model (including the effect of the diffusion capacitances for IGBT depletion layer (IGBT turn-off) and for depletion layer of the anti-parallel diode (diode turn-off)) and to the cable model (improved representation of the skin and proximity effect from [33] extended for capacitances also). The motor model is found to deliver satisfactory results and no further investigations are made in this direction, as this does not represent the purpose of this work. More details for the motor model are offered in a parallel work [54]. Finally the simulations results are in good agreement with the measurements at a self-built setup, presented in subchapter 3.1.

## 6.2 Methods for reduction of the parasitic effects

Using the simulation models previously developed and connected together, methods to reduce the parasitic effects (overvoltage and CM ground current) in electric drives with long feeders are investigated. The methods are dealing with changes in the gate drive control of the inverter (mainly the reduction of the output voltage slope) and impedance matching of the cable using filters. There are also methods to reduce the parasitic effects in the motor, e.g. the use of better stator winding insulation or isolated bearings, but they do not make the subject of this work.

First, Table 6.2 summarizes the investigated methods, related to the gate drive control,

**Table 6.2: Methods related to inverter for reduction of the HF parasitic effects**

	Variation of gate resistance $R_G$	2-step voltage rise		pre- and post-charge of cable stray elements
		with active driver	with 3-level converter	
Advantages/Disadvantages	+ very simple to implement – the switching losses increase proportional to the $R_G$ value	+ full control of the voltage slope and reduced sw. losses – complex drive circuitry and high sensitivity to the cable length	+ easy to implement – additional semiconductor devices necessary with afferent drive circuits	+ only software implementation necessary; reduces the value of the output choke – works only with inverter output chokes
Effects	only overvoltage reduction			
Switching energy / IGBT	12 mJ – turn on 13 mJ – turn off	7 mJ – turn on 8 mJ – turn off	–	–
Evaluation	unpractical	applicable for cable lengths < 30 m	applicable for cable lengths > 30 m	applicable only with output chokes

Table 6.3: Cable terminators used in electric drives with long feeders

		R filter	RC filter	RC Diode clamp filter	
				with Zener diodes	with DC-link feedback
Advantages/ Disadvantages		+ very simple to implement and to parameterize – very large losses due to the small resistance	+ simple to implement in Y or $\Delta$ configurations + simple parameterization – relatively high losses	+ voltage overshoot clamped with Zener diodes – relative high losses; power Zener diodes required	+ small losses due to a DC-link feedback – two additional cable conductors necessary to realize the DC-link feedback
Effects on HF phenomena		only overvoltage reduction			
Total losses	sim.	1411 W (22% ov.)	74 W (18.4% ov.)	81 W (22% ov.)	26.2 W (28% ov.)
	meas.	–	–	–	27.5 W (27% ov.)
Evaluation		unpractical	easy to implement and parameterize	not optimal due to power Zener diodes	good solution due to the low losses

Table 6.4: Inverter output filters used in electric drives with long feeders

		RL filter	RLC filter	RL Diode clamp filter
Advantages/ Disadvantages		+ few passive elements – larger inductor values than other topologies necessary for the same results	+ the additional capacitance allows a reduction of the inductor for same results – relative high resistive losses	+ voltage overshoot at filter output clamped by diodes to the DC-link level – additional connections to the DC-link P and N rails
Effects on HF phenomena		reduction of overvoltage and CM ground current		
$R_F$ losses (sim.)		–	214 W (25.6% ov.)	34.4 W (23.5% ov.)
Evaluation		simple to implement, they are used in practice; attention needed for the design of the output chokes	mostly used in industry; depending on the cutoff freq. they classify in dV/dt filters or Sine-Wave filters	good solution: like the RC diode-clamp terminator, low resistive losses due to the energy feed-back to DC link

together with their evaluations. While the simple variation of the gate resistance  $R_G$ , to decrease the voltage slope, leads to proportional increase of the losses with resistance value, other methods, like splitting the voltage slope in two parts and controlling the delay between these individual steps, determine lower losses. Depending on the cable length, the active drive or the 3-level converter solutions can be applied. Another method deals with pre- and post-charging of the stray elements of the cable, but it can be implemented only with additional inverter output chokes.

The second type of methods to reduce the parasitic effects, used in electric drives with long feeders, are related to cable. For that, filters are used either at the motor side (cable terminators) or the inverter side (inverter output filters). While the cable terminators are based on the cable impedance matching, the inverter output filters reduce the voltage slope at the inverter output, thus changing the condition for overvoltage at the motor terminals (see Eq. 2.29 and Eq. 2.30 from section 2.2.2). An overview of both filter types is given in Table 6.3 and Table 6.4. Although additional semiconductor devices are needed to build the diode bridge, the RC-diode clamp terminator and the RL-diode clamp output filter represent an optimal solution, because the energy is fed back to the DC link. Considering the trend from the last decade, that the costs are decreasing for semiconductors and are remaining constant for passive elements, these optimal solutions are a good alternative to the RC cable terminator and/or the RLC output filter, respectively.

A thorough examination (especially for losses) of the filter topologies can be further conducted by including better simulation models of the filter components.

**Table 6.5: Comparisons of HSI with output filters and QR DC-link converter**

	<b>HSI + <math>dV/dt</math> filter</b>	<b>HSI + SineWave EMC</b>	<b>QR DC-link converter</b>
<b>Advantages/ Disadvantages</b>	+ no additional connections to DC link required – overvoltage rest – relative high losses	+ reduced motor losses + sinusoidal line-line and line-earth voltages – unfit for high dynamic – high coupling to earth	+ no output filter required + total separation from DC link during resonant period – complex control of resonant cycle
<b>Effects on HF phenomena</b>	overvoltage and CM ground current reduction	overvoltage and CM ground current reduction line-earth voltage reduction	overvoltage and CM ground current reduction CM voltage reduction
<b>Efficiency (<math>P = 3.14</math> kW)</b>			
<b>Evaluation</b>	convenient solution when no big restrictions for HF parasitic effects are used	good solution if high dynamic is not required	represents a good compromise between the other two solutions (more parasitic effects reduction than $dV/dt$ filter for less losses and good dynamic)

### 6.3 Quasi-resonant converter topology

The last part of this work deals with the implementation of a quasi-resonant converter topology in electric drives with long cables. Using additional passive elements and switches, a resonant operation can be initiated from user (PWM-compatible). During this resonant period, the PWM state of the inverter bridge can be changed under ZVS condition, while the voltage of the inverter bridge, i.e. the voltage seen by motor at the inverter output, is zero. In fact, two important aspects are analyzed in parallel:

- the high efficiency characteristic of the converter is achieved using an active control of the resonant period to store in the passive elements only the necessary amount of energy that allows restoring the voltage of the inverter bridge at the end of the resonant cycle. Also, state-of-the-art switches are used to increase the efficiency of the converter.

- the motor friendly characteristic refers to the milder voltage slopes at the inverter output, as they depend in this case only on the passive elements and no longer on the hard-switched semiconductors (e.g. the passive elements were designed to obtain a 20% overshoot at the motor terminals using a 34m-long cable). A second aspect of this characteristic is the use of a second switch to completely separate the inverter bridge from the DC link. Thus, during the resonant operation, which is used also as a zero-vector period in a DSC-like modulation technique, the CM voltage is reduced to zero (instead of  $V_{DC}/2$  level in common SV-PWM), leading to a reduction or even elimination of the bearing currents.

Finally, the QR DC-link converter was tested and compared to the hard-switched inverters (HSI) equipped with output filters on the basis of a similar reduction of the HF parasitic effects. The conclusions are summarized in Table 6.5. The QR DC-link converter combines the advantages of both filters: reduces the overvoltage and the CM voltage (responsible for the bearing currents) with fewer losses than the  $dV/dt$  filter. Still, the cable length, that can be used, is restricted by the imposed voltage slope (i.e. the design of the resonant circuit).

Improvements to the QR DC-link converter, regarding the reduction of the losses, need to be researched further: use of new semiconductor devices (SiC JFET) and design improvement of the resonant inductor. Also different implementation/topologies for the QR DC-link converter with the same effect on the HF parasitic phenomena and improved efficiency have to be considered.



## 7 Appendix

### 7.1 Cable parameters

Following, the parameters for the studied cables are detailed.

#### 7.1.1 LAPP Classic 115CY

##### Characteristics

Number of conductors	5
Conductor cross-section	2.5 mm <sup>2</sup>
Shielded	Yes
Length	34 m

In Figure 7.1 (a), the cross-section of the cable is illustrated. The dimensions are:  $d_1 = 8.1$  mm,  $d_2 = 3$  mm,  $d_3 = 1.6$  mm, shield thickness  $d_4 = 0.4$  mm and thickness of the PVC external jacket  $d_5 = 1.15$  mm.

##### Parameters

Table 7.1 summarizes the cable parameters obtained using three different methods. It can be noticed that the difference between the analytically calculated and measured parameters is relative high due to adopted simplifications (homogenous space between conductors with constant permittivity; proximity effect only between two neighbored conductors) and high geometrical complexity (5 conductors plus shield). Although the FEM calculations deliver better results in this case, still the analytical results can be accepted.

Table 7.1: Parameters for the LAPP Classic 115CY cable

	$C_A$ / pF/m	$C_B$ / pF/m	$C_C$ / pF/m	$L_A$ / nH/m		$L_B$ / nH/m	
				LF	HF	LF	HF
Analytical	167	380	279	560	471	816	596
Measured	187	399	291	639	421	815	472
FEM	189	435	-	634	408	826	466

Further, to simulate the frequency dependency of the cable parameters, two methods, based on the ladder equivalent circuit, were presented in section 2.2.5 [52] and subsection 3.2.2.1 [33]. The parameters for the ladder circuits are presented in Table 7.2 for both methods. The second method has as inputs the measured values of the parameters for a chosen frequency range, i.e. the phase inductance and resistance  $L'$ ,  $R'$  and the partial

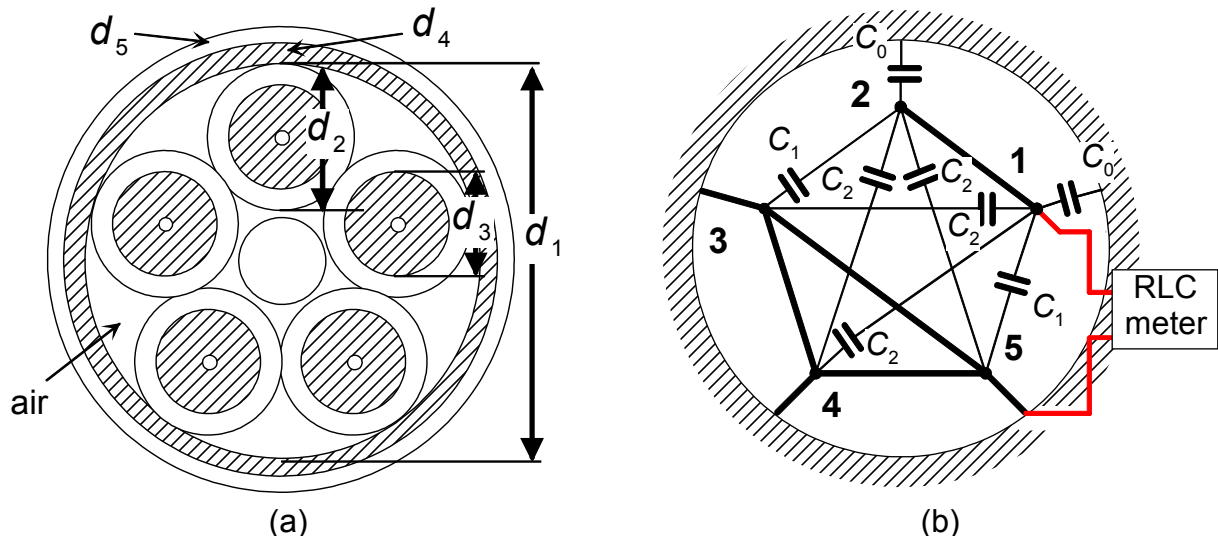
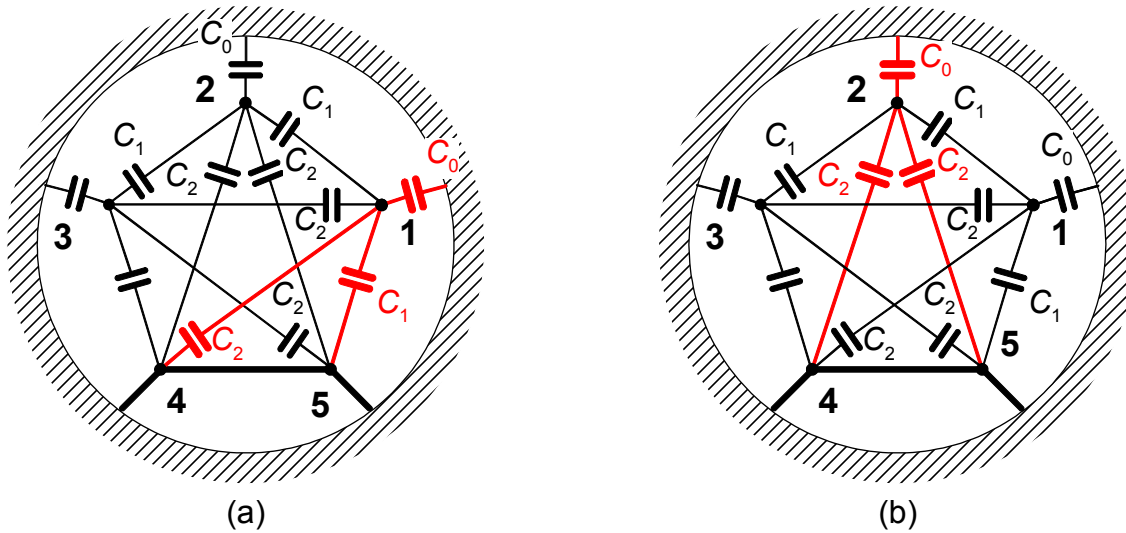


Figure 7.1: Cable cross-section (LAPP) (a) and measurement setup for  $C_c$ (b)



**Figure 7.2: Equivalent conductor-earth capacitance connection  $C_{ech\_1-0}$  (a) and  $C_{ech\_2-0}$  (b)**

capacitances  $C_0$ ,  $C_1$  and  $C_2$ . It is possible to obtain these capacitances from measurements only if a third measurement setup is used, see Figure 7.1 (b). In this case, two conductors are short-circuited, e.g. conductor 1 and 2, and the equivalent capacitance is measured with respect to the remaining three connected together and to shield. The other two measurement configurations were detailed in subsection 2.2.3.3, Figure 2.30 (a) and (b). Thus, the equivalent capacitance  $C_C$  is obtained and the following system of equations can be expressed by including the expressions for the other two equivalent capacitances  $C_A$  and  $C_B$ :

$$C_A = C_0 + 2C_1 + 2C_2$$

$$C_B = 3C_0 + 2C_1 + 4C_2$$

$$C_C = 2C_0 + 2C_1 + 4C_2$$

Eq. 7.1

Solving this equation system, the partial capacitances can be calculated as follows:

$$C_0 = C_B - C_C$$

$$C_1 = (2C_A - C_C) / 2$$

$$C_2 = (2C_C - C_B - C_A) / 2$$

Eq. 7.2

### Equivalent conductor-earth capacitances

Because the two remaining conductors are connected to the shield (4<sup>th</sup> conductor and PE), the line-ground capacitance is no longer represented only by  $C_0$ . In Figure 7.2, the partial capacitances of the entire system are shown. It can be noticed that the equivalent capacitances  $C_{ech\_1-0}$  and  $C_{ech\_3-0}$  are determined by all three partial capacitances  $C_0$ ,  $C_1$  and  $C_2$  (see Figure 7.2 (a)) whereas  $C_{ech\_2-0}$  only by  $C_0$  and  $C_2$  (see Figure 7.2 (b)).

**Table 7.2: Ladder circuit parameters for skin and proximity effect (LAPP cable)**

Index	Method from [52]		Method from [33] (6 branches)					
	$L_{Ax}$	$R_{Ax}$	$L_{Ax}$	$R_{Ax}$	$C_{1x}$	$G_{1x}$	$C_{ech\ 1-0\ x}$	$G_{ech\ 1-0\ x}$
	nH/m	$\Omega$ /m	nH/m	$\Omega$ /m	pF/m	$\mu$ S/m	pF/m	$\mu$ S/m
1	26.4	0.587	4676	0.131	5.13	0.0018	10.7	0.0015
2	84.4	0.252	171.5	0.0332	3.45	0.004	0.9	0.1846
3	270	0.108	114.5	0.058	3.1	0.09	8.47	0.23
4	-	0.046	94.94	0.135	2.63	0.85	7.34	2.46
5	-	-	55.3	0.570	1.87	11.5	6.52	25.16
6	-	-	345.4	15.13	31.38	104.9	124.44	467.02

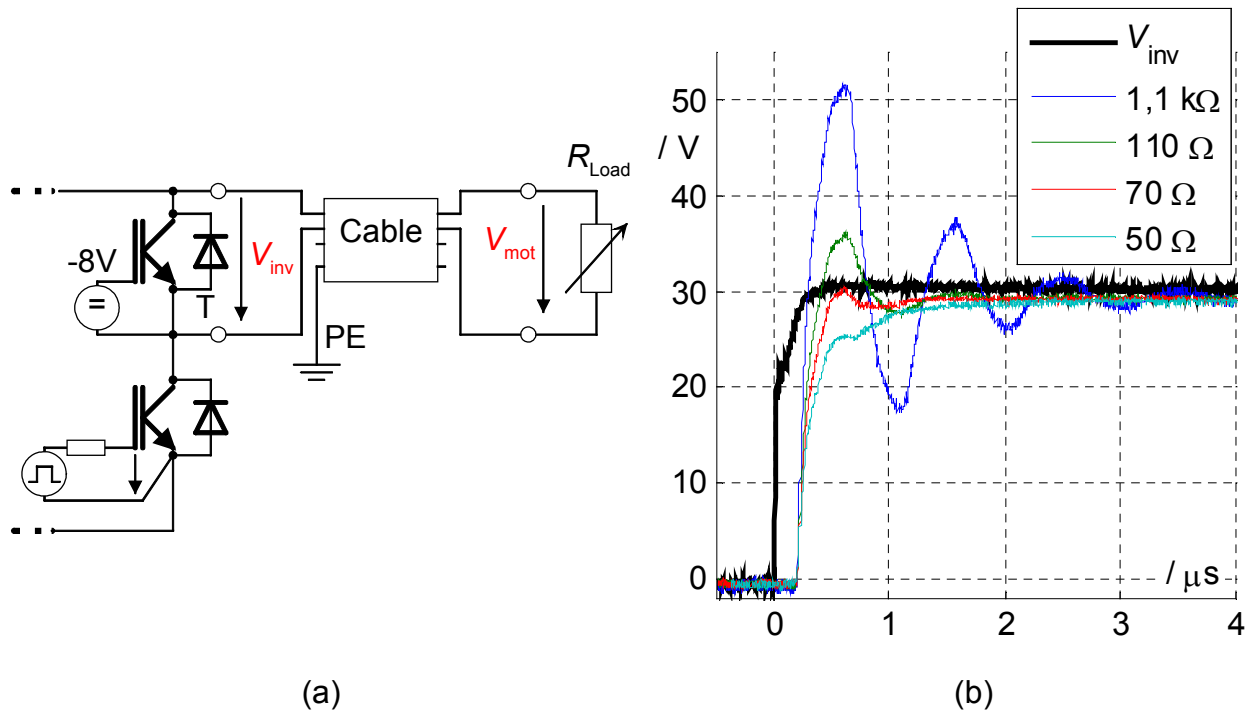


Figure 7.3: Measurement setup (a) and waveform (b) for the run-time impulse method

Following relations are used in this case:

$$C_{ech\_1-0} = C_{ech\_3-0} = C_0 + C_1 + C_2 \text{ and } C_{ech\_2-0} = C_0 + 2 \cdot C_2. \quad \text{Eq. 7.3}$$

After calculating the values of the equivalent capacitance from measurements, they are used as inputs for the calculation algorithm of the ladder circuit parameters from [33]. The obtained values are listed in Table 7.2.

### Phase inductance and capacitance

The most important parameters, to calculate the time and speed of the wave propagation across the cable, are the phase inductance  $L'$  and capacitance  $C'$ . These quantities are closely related to the chosen cable configuration, especially at cables with more than three conductors. The importance of the chosen conductor pair has been already shown in the sections 2.2.3 and 2.2.4.

A practical method to obtain the propagation time of the voltage wave is the run-time impulse method, which consists in injecting a low-voltage impulse on the cable using the inverter and having a variable resistance connected at the load side, like in Figure 7.3 (a) shown. This method was used in [53] to check the results for  $L'$  and  $C'$ . By varying the resistance, the cable impedance  $Z_C$  is matched when no reflections occur. Then, the propagation time  $t_p$  is read from the plotted voltage waveforms at the inverter and motor cable ends, see Figure 7.3 (b). The wave velocity can be easily determined from Eq. 2.24 (page 27) if the total length  $l_{total}$  of the cable is known. Using the same equation plus the

Table 7.3: Per phase parameters and wave propagation delay and speed (LAPP cable, 34m)

	Conductor 1 – 0 (CM)					Conductor 2 – 0 (CM)				
	$C'$	$L'$	$t_p$	$v_C$	$Z_C$	$C'$	$L'$	$t_p$	$v_C$	$Z_C$
	pF/m	nH/m	ns	m/μs	Ω	pF/m	nH/m	ns	m/μs	Ω
Analytical	162	-	-	-	-	158	-	-	-	-
Measured	164	262	223	153	40	163	260	221	154	40
	Conductor 1 – 2 (DM)					Conductor 1 – 3 (DM)				
	$C'$	$L'$	$t_p$	$v_C$	$Z_C$	$C'$	$L'$	$t_p$	$v_C$	$Z_C$
	pF/m	nH/m	ns	m/μs	Ω	pF/m	nH/m	ns	m/μs	Ω
Analytical	96	471	229	148	69.9	86.7	596	244	139	83
Measured	92	460	220	154	70	71	575	217	156	90

impedance equation  $Z_C \approx \sqrt{L'/C'}$ , the values for  $L'$  and  $C'$  can be calculated. Due to the complex structure of the LAPP cable (5 cond.), the phase inductances and capacitances will always depend on the pair of conductors, chosen to apply the voltage impulse.

The values for measured propagation time  $t_p$ , wave speed  $v_C$  and the calculated  $L'$  and  $C'$  are listed in Table 7.3 for different conductor pairs. In reversed order, knowing the values for the partial capacitances, self and mutual inductances (analytically determined), the phase quantities may be calculated and finally the wave propagation velocity and cable impedance estimated. However, due to the complex geometrical configuration, the phase inductance between one conductor and shield is difficult to calculate analytically and therefore will not be considered further.

From Table 7.3, the influence of the cable shield can be observed: the phase capacitance between conductor 1 and shield (0) is much higher than between conductor 1 and 2. However, the phase inductance will compensate and the wave propagation speed remains almost constant. On the contrary, large differences, regarding the cable impedance, are observed between the two configurations.

### 7.1.2 Ozoflex H07RN-F

#### Characteristics

Number of conductors	4
Conductor cross-section	4 mm <sup>2</sup>
Shielded	No
Length	99 m

In Figure 7.4 (a), the cross-section of the cable is illustrated. The dimensions are:  $d_1 = 10.3$  mm,  $d_2 = 4.3$  mm,  $d_3 = 2.3$  mm and thickness of the external jacket  $d_4 = 1.9$  mm.

#### Parameters

Table 7.4 summarizes the cable parameters obtained using three different methods. The analytical results are more close to measurements in this case, because the external jacket fills almost completely the space between conductors, leading to a homogenous space. Also here, the complexity is significantly reduced, having only four conductors and no shield.

The frequency dependence of the cable parameters is modeled using the same methods presented before. The ladder circuit parameters are summarized in Table 7.5. An

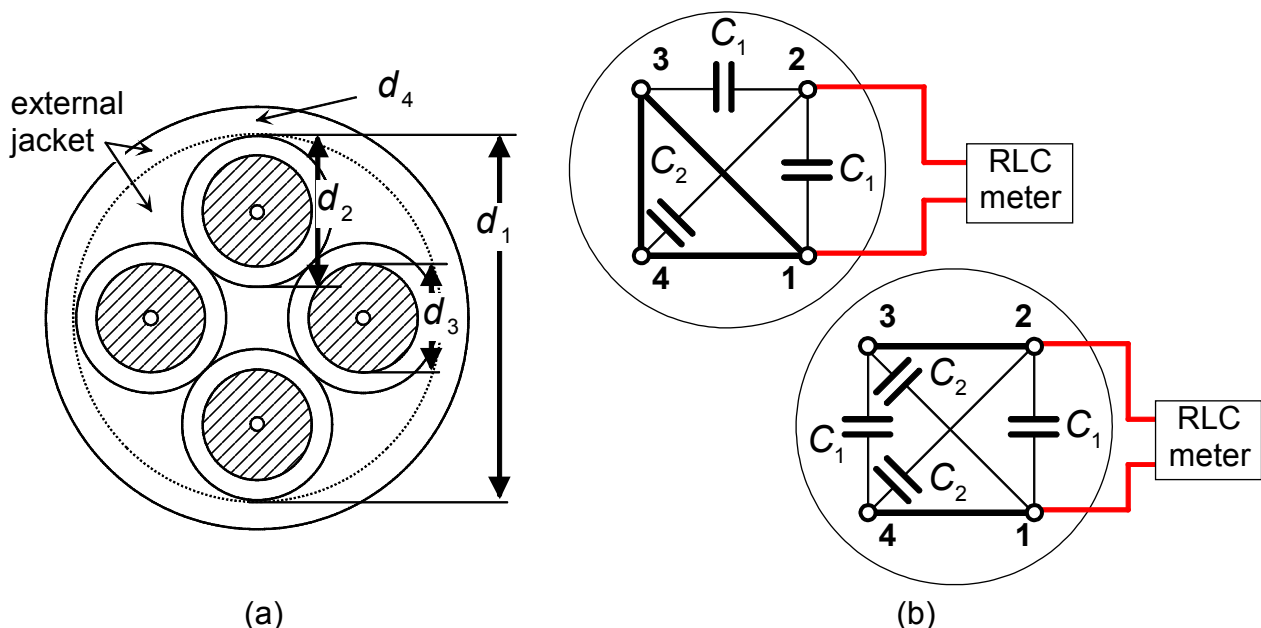


Figure 7.4: Cable cross-section (Ozoflex) (a); measurement setup for  $C_A$  and  $C_B$  (b)

**Table 7.4: Parameters for Ozoflex H07RN-F cable**

	$C_A$ / pF/m	$C_B$ / pF/m	$L_A$ / nH/m		$L_B$ / nH/m	
			LF	HF	LF	HF
Analytical	127.8	131.5	683.5	583.5	822.1	722.1
Measured	117	129	753	641	875	744

**Table 7.5: Ladder circuit parameters for skin and proximity effect (Ozoflex cable)**

Index	Method from [52]		Method from [33] (4 branches)					
	$L_{Ax}$ LD	$R_{Ax}$ LD	$L_{Ax}$	$R_{Ax}$	$C_{1x}$	$G_{1x}$	$C_{2x}$	$G_{2x}$
	nH/m	$\Omega$ /m	nH/m	$\Omega$ /m	pF/m	$\mu$ S/m	pF/m	$\mu$ S/m
1	19.08	0.424	4538	0.089	4	0.0012	2.02	0.0015
2	66.48	0.168	106	0.0155	3.23	0.034	1.73	0.026
3	231.66	0.066	70.35	0.071	3.62	2.47	1.56	0.865
4	-	0.26	600.26	0.7673	45.47	101.03	9.53	23.05

important simplification for this case represents the missing of the conductor-shield capacitance  $C_0$ . To determine the two partial capacitances  $C_1$  and  $C_2$ , necessary to calculate the ladder parameters from [33], only two measurements are required, as shown in Figure 7.4 (b). From the obtained equivalent capacitances  $C_A$  and  $C_B$ , the partial capacitances are calculated by solving following equation system:

$$C_A = 2C_1 + C_2$$

$$C_B = 2C_1 + 2C_2$$

Eq. 7.4

and obtaining following relations:

$$C_1 = (2C_A - C_B) / 2$$

$$C_2 = C_B - C_A$$

Eq. 7.5

### **Equivalent conductor-earth capacitances**

Because the shield is missing in this case, the 4<sup>th</sup> conductor is used for the earth connection, thus simplifying the conductor-earth capacitance:

$$C_{ech\_1-0} = C_{ech\_3-0} = C_1 \text{ and } C_{ech\_2-0} = C_2.$$

The parameters for the ladder circuits are listed in Table 7.5. For the algorithm from [33], a four-branch ladder circuit was chosen because the simulation results are good and lead to less simulation time than the six-branches model.

### **Phase inductance and capacitance**

In a similar way, the propagation delay  $t_p$  and speed  $v_C$  of the voltage wave are determined using the run-time impulse method. Knowing the total cable length, the phase inductance and capacitance are calculated, using Eq. 2.24 and the expression of the cable impedance  $Z_C$ . An essential simplification for this case represents the missing of the shield. Thus, the equivalent capacitance between conductor 1 and 0 is equal to the capacitance between two neighbored conductors. Table 7.6 summarizes the values determined by measurements and analytical calculations, where a very good agreement is observed due to the more simple cable construction and configuration.

**Table 7.6: Per phase parameters and wave propagation delay and speed (Ozoflex cable, 99m)**

	Conductor 1 – 2					Conductor 1 – 3				
	$C'$	$L'$	$t_p$	$v_C$	$Z_C$	$C'$	$L'$	$t_p$	$v_C$	$Z_C$
	pF/m	nH/m	ns	m/ $\mu$ s	$\Omega$	pF/m	nH/m	ns	m/ $\mu$ s	$\Omega$
Analytical	86	584	701	141	82.3	66	722	682	145	105
Measured	72	582	640	155	90	59	716	644	154	110

### 7.1.3 Motorflex YSLYCY-JZ

#### Characteristics

Number of conductors	4
Conductor cross-section	6 mm <sup>2</sup>
Shielded	Yes
Length	100 m

In Figure 7.5, the cross-section of the cable is illustrated. The dimensions are:  $d_1 = 14.6$  mm,  $d_2 = 5.2$  mm,  $d_3 = 2.8$  mm, thickness of the internal PVC jacket  $d_4 = 1$  mm, shield thickness  $d_5 = 0.5$  mm and thickness of the external PVC jacket  $d_6 = 2$  mm.

#### Parameters

Table 7.7 summarizes the cable parameters obtained, using three different methods. In this case the difference between the analytical calculations and measurements are again high due to the higher complexity of the system (presence of shield). Moreover, the FEM calculations are also offering different results, especially regarding the cable inductances.

Because this cable was not directly available at the SRT institute, the variation of the frequency parameter could not be analyzed in detail.

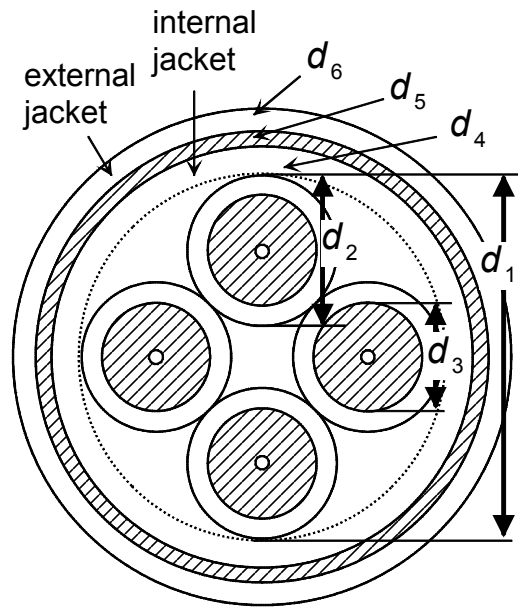


Figure 7.5: Cable cross-section (Motorflex)

Table 7.7: Parameters for Motorflex YSLYCY-JZ cable

	$C_A$ / pF/m	$C_B$ / pF/m	$L_A$ / nH/m		$L_B$ / nH/m	
			LF	HF	LF	HF
Analytical	202	386	571	546.7	765	689.7
Measured	229	497	620	470	760	534
FEM	206	422	544	382	682	444

## 7.2 Motor parameters

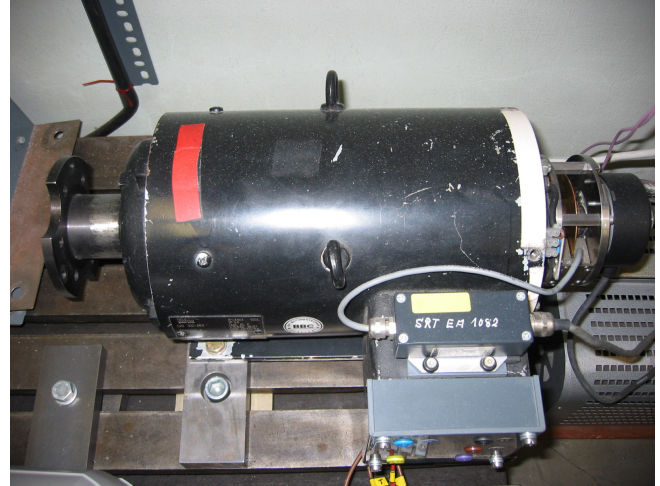
Following electric machines were used to test the inverter-cable-motor system.

### 7.2.1 BBC (ABB) QS100-3B3 induction machine

The motor details are summarized, together with the parameters of the HF equivalent circuit, in Table 7.8. A picture of this motor is shown in Figure 7.6. The CM and DM input impedance measurements were already illustrated in Figure 2.37 from section 2.3.3.

**Table 7.8: BBC 5-kW induction motor parameters**

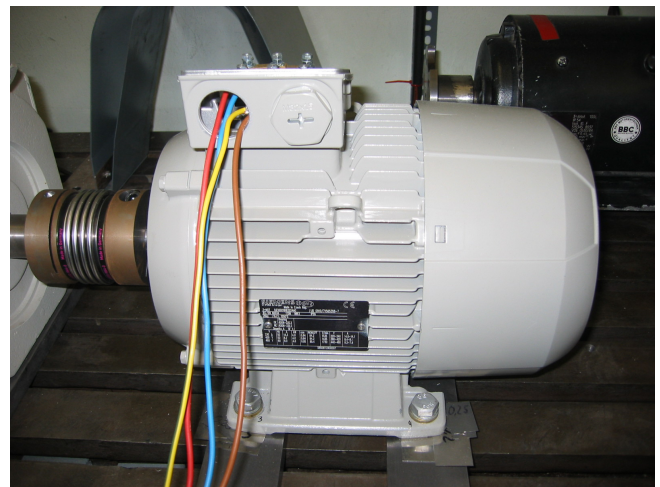
Rated power / kW	5
Rated torque / Nm	32.5
Rated current / A	17 rms
Magnetizing current / A	14 rms
Rated voltage / V	330 rms (Y)
Rated speed / 1/min	≈1500
Max. speed / 1/min	7000
$\cos \varphi$	0.65
Pole pairs	2
$L_{CM}$ / mH	0.26
$L_{DM}$ / mH	3.48
$C_{res1}$ / nF	1.27
$R_{res1}$ / $\Omega$	6.06
$C_{res2}$ / nF	2.8
$R_{res2}$ / $\Omega$	263.7
$R_{fe i}$ / $\Omega$	2520
$L_{ph i}$ / mH	1.81
$M_{ij}$ / mH	-0.51
$L_{con}$ / $\mu$ H	0.315



**Figure 7.6: BBC 5kW induction motor**

**Table 7.9: Siemens 4-kW IM parameters**

Rated power / kW	4
Rated torque / Nm	27
Rated current / A	8.4 rms
Magnetizing current / A	4 rms
Rated voltage / V	400 rms (Y)
Rated speed / 1/min	1435
$\cos \varphi$	0.84
Pole pairs	2
$L_{CM}$ / mH	0.332
$L_{DM}$ / mH	36.9
$C_{res1}$ / nF	0.4
$R_{res1}$ / $\Omega$	5.15
$C_{res2}$ / nF	4.52
$R_{res2}$ / $\Omega$	894
$R_{fe i}$ / $\Omega$	5428
$L_{ph i}$ / mH	16.7
$M_{ij}$ / mH	-7.87
$L_{con}$ / $\mu$ H	0.5



**Figure 7.7: Siemens 4kW induction motor**



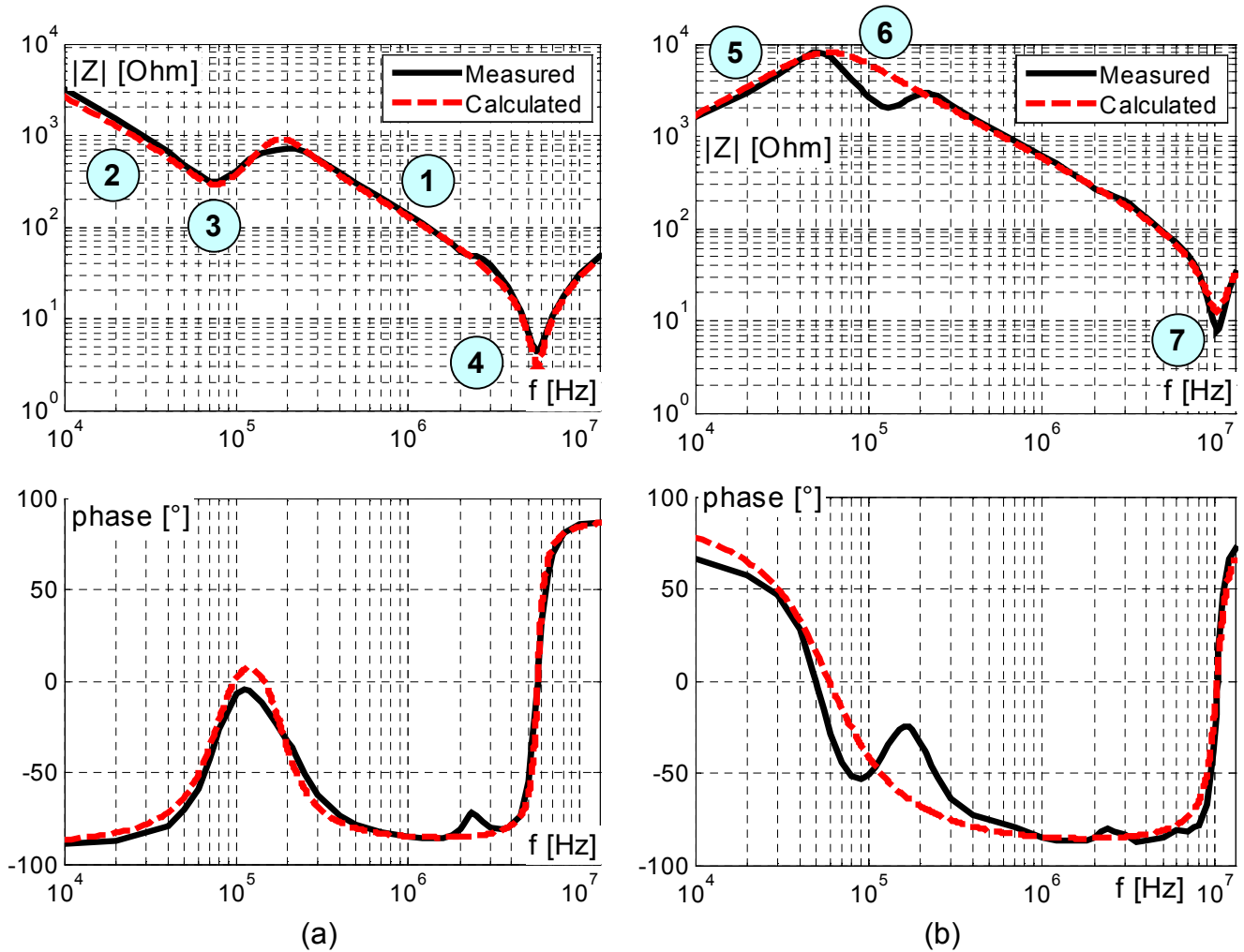


Figure 7.8: Impedance amplitude and phase frequency characteristic for CM (a) and DM (b)

Because this electrical machine is designed for high speeds, a high magnetizing current (app. 80% from the nominal current) is necessary to build the nominal flux. On one hand, the high nominal flux allows reaching high speeds when the flux reduction is used. On the other hand, a high magnetizing current increases the inverter losses. Therefore, an ordinary induction motor was preferred to this motor when the QR inverter was implemented. Lower magnetizing current allows resonant operation with less inverter losses. Such an induction motor is presented in the next section

### 7.2.2 Siemens 1LE10021BB222AA0 induction motor

This is an ordinary commercial induction motor, built for industrial applications (low cost and relative high efficiency). The motor details are summarized in Table 7.9 together with the parameters of the HF equivalent circuit. A picture of this motor is shown in Figure 7.7.

The measurements and computations of the CM and DM input impedance are illustrated in Figure 7.8. Using the mathematical relations from Eq. 2.51 to Eq. 2.56, the HF model parameters are determined from measurements. In a similar way, the important points of interest are marked on the modulus characteristic (both CM and DM measurements). It is noticeable a same variation tendency of the of the machine input impedance, depending on frequency:

- in CM, the capacitive effect is dominant up to frequencies of app 5MHz. Here, the effect of the stray inductances from the connection wires starts to dominate. Around 100 kHz, the effect of the phase stray inductance is noticed in a resonance and anti-resonance pair. Before this frequency, both capacitances  $C_{res1}$  and  $C_{res2}$  contribute to the impedance behavior. After 200 kHz, only the



**Table 7.10: Piller 15-kW DC motor parameters**

Rated power / kW	15
Rated current / A (armature)	43
Rated voltage / V (armature)	400
Rated / Maximum current / A (excitation)	0.85 / 2.5
Rated / Maximum voltage / V (excitation)	70 / 220
Rated / Maximum speed / 1/min	3250 / 8000

**Figure 7.9: Piller 15kW DC motor**

input capacitance  $C_{res1}$  is dominant, because the phase stray inductance cuts the HF current.

- for the DM test, the effect of the mutual inductance between phases is dominant up to app. 50 kHz. Beyond this frequency, the effect of the input capacitance  $C_{res1}$  starts to dominate the capacitive behavior of the input impedance. This behavior is maintained for frequencies up to 10 MHz where, the effect of the stray inductance from the connection wires starts to be dominant.

After obtaining the HF model parameters, the equivalent impedance of the HF model from Figure 2.35 is calculated depending on the frequency. The results are plotted together with measurements in Figure 7.8. A good approximation of the measurements is observed. However, a slight deviation is observed for the DM connection around 100 kHz, due to the additional parasitic effects that have been neglected. These can be considered if auxiliary components are added to equivalent circuit [36]. However, this leads to unnecessary increase of the complexity and, therefore, will not be further considered.

### 7.2.3 Piller GML 112.17V DC motor

This is a DC machine with brushes and a separate excitation, used as a generator to load the investigated induction motor. The DC generator parameters are summarized in Table 7.10. A picture of this motor is shown in Figure 7.9. Due to the relative high excitation current, an external ventilator is used to cool the excitation winding.



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## Academic Profile

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